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Dynamic Hardware Adaptation for Multichannel Neurophysiological Feature Extraction

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Abstract

The multichannel neurophysiological signal processing systems should have to meet strict and usually competing criteria connected with the latency, throughput and power performance along with adaptability. In real-world electroencephalography (EEG), electromyography (EMG), and electrocardiography (ECG) recording and acquisition, channel counts, quality of signals, and complexity of feature ideation are major challenges to pipeline software and hardware accelerators with fixed functionalities. These traditional methods do not possess the ability to be flexible so that they can easily meet dynamic workloads without compromising on real-time performance. This article has described a dynamically reconfigurable multichannel neurophysiological feature extraction hardware architecture based on an FPGA platform and intended to be used to facilitate adaptive and high-energy-efficiency real-time processing. The given architecture uses the capabilities of runtime partial reconfiguration to allocate computational resources in a dynamic manner due to the number of active channels, as well as the assigned task(s) and the task(s) to perform a specific feature extraction. It implements a single processing architecture to enable time-domain, frequency-domain and timefrequency feature extraction in the same reconfigurable platform. The feature extraction modules can be changed dynamically without disrupting the flow of operation of the system, hence dynamic capability to adapt to varying requirements of the signals and application. The implementation and evaluation of the architecture is done on the basis of a field-programmable gate array (FPGA) platform under realistic multichannel neurophysiological workloads. The experimental performance is better in terms of utilizing the available hardware resources and lowering energy consumption than the energy consumption of fixed FPGA-based designs, and maintains deterministic low-latency performance. These findings affirm that dynamic partial reconfiguration is a feasible idea to scalable and power efficient neurophysiological signal processing. The suggested architecture offers a versatile hardware base of future generation real-time brain-computer interfaces, wearable biomedical systems, and adaptive neuro-monitoring software.

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Introduction

The standard of the modern brain computer interface, wearable health technologies, and real-time health monitoring systems include neurophysiological interfaces, including electroencephalography (EEG) or electromyography (EMG) and electrocardiography (ECG). In an effort to enhance spatial resolution, signal strength and diagnostic quality, modern acquisition systems have been turning more and more to multichannel sensing architectures, which typically include tens and hundreds of parallel signal channels. As much as multichannel configurations are known to increase system capability, they create high data rates, and introduce high computational and energy burden especially in the feature extraction stage, which directly influences the accuracy of classification, latency and overall system efficiency.[1, 2] The traditional software-based process pipelines that are designed to run on a general-purpose processor or embedded CPU have an advantage of providing algorithmic flexibility but have difficulty meeting strict real-time and power requirements in portable and wearable systems.[3] On the other hand, some hardware accelerators (usually fixed-function) implemented on application-specific integrated circuits (ASICs) or fixed FPGA designs can offer high throughput and low latency but cannot be reconfigured when the number of channels, or signal quality or other features to extract changes during operation.[4, 5] In the real world dynamic situation, this rigidity contributes to inefficient use of resources and unneeded consumption of energy. Computing Reconfigurable computing with FPGA based computing, in particular with runtime partial reconfiguration, provides a promising option by providing a combination of hardware-capable performance and post-deployment flexibility.[6, 7] Toggling can be done dynamically, with runtime system reconfiguration permitting hardware modules to be switched in or out, modified, or replaced, without affecting the operation of the system so that computational resources can be dynamically allocated according to the current workload. Nonetheless, the majority of the current neurophysiological processing frameworks on FPGA utilise fixed architectures and fail to completely utilise run-time reconfigurability to tailor feature extraction pipelines to run-time feature count or chosen subsets of features.[8]

In order to overcome these constraints, the paper will present a proposed FPGA-based hardware architecture, which is dynamic and reconfigurable to get multichannel neurophysiological features extraction. The proposed design facilitates time-domain, frequency-domain and time-frequency feature extracted functionality, in a single modular system and runtime partial reconfiguration to dynamically change processing capability. It is evaluated in a comprehensive experimental study to determine the performance, resource utilisation, and energy efficiency as compared to the static designs using FPGa.

The rest of this paper follows a structure in the following way. Standard 2 presents related literature, in the areas of hardware-accelerated neurophysiological signal processing and reconfigurable computing. The proposed architecture and reconfiguration strategy is presented in Section 3. Section 4 explains the implementation and experimental set up. Section 5 talks about the performance evaluation and results. Lastly, there is a conclusion of the paper that spells out the direction of future research in Section 6.

Related Work

Neurophysiological signal processing Hardware acceleration of neurophysiological signal processing has been a popular research area to tackle the highly real-time and energy limiting factors of EEG, EMG and ECG hardware. The first FPGA-based models were mainly dedicated to time-domain feature extraction using fixed-function pipelines, spectral analysis (fast fourier transform (FFT)) and computation of the discrete wavelet transform (DWT). These designs have deterministic low-latency performance, and high throughput, but commonly require a fixed number of input channels, and special purpose pipelines of feature extractions, which makes them less able to adapt to dynamic acquisition contexts.[9, 10] In order to enhance adaptability, some works have discussed the configurable or parameterized hardware architectures where feature selection or channel routing is programmed/configured by means of software or by register/register configuration. Such solutions are not very flexible, but they are based on fine-grade reconfiguration or time-multiplexing of resources that can be a source of low resource usage and high power usage when runtime requirements vary among systems.[11, 12] Additionally, these architectures do not enable the underlying hardware architecture to be reconfigured dynamically which limits their ability to scale effectively as the number of channels changes or the

feature heterogeneity. Dynamic partial reconfiguration (DPR) of FPGAs has become an influential approach in order to provide the ability to modify the functionality of a hardware at runtime and not to disrupt the functionality of a system. DPR has been effective in areas like software defined radio, video processing, and adaptive signal processing to provide functional swapping and power sensitive operating.[13] Its use in multichannel neurophysiological feature extraction architectures, however, remains little used, most available biomedical FPGA designs to date still depending on statical architecture or offline reconfiguration.

Unlike the previous literature, the suggested architecture explicitly incorporates the facility of runtime partial reconfiguration so that fine-grained, on-need adaptation of feature extraction modules can take place, contingent on the active number of channels in addition to the belongings of feature types of choice. The proposed method overcomes some of the main shortcomings of the current systems with regard to scalability and resource efficiency as well as energy consumption and maintains deterministic real-time performance by integrating modular hardware design with DPR.

System Overview

Target Application Scenario

The suggested study is focused on the dynamic real-time multichannel neurophysiological signal processing applications where the number of active channels and the tasks that have to be performed to extract the features during the system operation can be affected dynamically. This variability is a typical feature of adaptive systems based on electroencephalography (EEG) brain electrodes interfaces (BCI), wearable health devices, and long-term neuro-monitoring utility, where signal quality, state of the user or the application suitability and energy availability varies or dictates processing needs. The issue with a fixed processing pipeline, in such cases, is that it is a waste of resources and which causes needless power usage, when there are less channels in use, or when a simpler set of features are used. The study is thus performed on the premise that a good acceleration hardware should be able to achieve the ability of runtime flexibility but maintain non-random low-latency processing. This prompts the utilisation of reconfigurable hardware that has the capability to alter its feature extraction functionality when not compromising the possibility of data acquisition.

Architecture Overview

The proposed system is deployed in a FPGA-based system-on-chip (SoC) platform to be implemented and configured into a fixed and dynamically reconfigurable area as shown in Fig. 1. Its part is the continuous operation of the system and stored in the static region consists of sensor data acquisition interfaces, input buffering, control logic, and communication with external memory or host processors. This part also contains a runtime manager checking the status variables of a system, including number of running channels, chosen feature sets and power budget. The reconfigurable region contains hardware feature extraction modules which can be loaded or swapped in at runtime by partial reconfiguration. The streaming sensor information is directed out of the stationary section into the active feature extraction section that is currently working and is operated in real time and sent back to the stationary part to be stored or sent. The system can recover the continuous operation through the reconfiguration of control and data acquisition logic in the static region, thereby maintaining the continuous operation of the system.

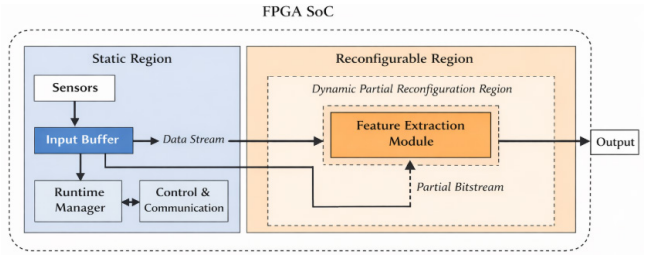

Fig. 1: FPGA-Based System Architecture with Static and Dynamically Reconfigurable Regions

Proposed FPGA system architecture block diagram depicting the fixed part of the system, dynamically reconfigurable part feature extraction part and dynamic partial reconfiguration controller of multichannel neurophysiological signal processing.

Dynamic Reconfigurable Feature Extraction Architecture

Modular Feature Extraction Design

The feature extraction functionality is achieved with hardware block implementation in which every hardware block is modular, and is capable of computing a certain type of neurophysiological features. The study takes three areas of widely used features into consideration namely: time-domain, frequency-domain, and time frequency features. Every module is

executed in the form of a parameterizable datapath, which takes streaming input samples.

Let $x_c[n]$ denote the discrete-time signal sample from channel c. A generic feature extraction operation can be expressed as

$$f_c = F(x_c[n]) \quad (1)$$

where F(·) represents the selected feature computation function, such as mean, variance, spectral power, or wavelet coefficients. Each of the feature modules has a standardised input/output interface, which enables them to be integrated directly into the reconfigurable region, and be replaced without changing the static control logic.

Runtime Reconfiguration Strategy

Dynamism partial reconfiguration (DPR) is used to allow replacement of feature extraction modules during runtime, and still allow the system to operate, as shown in Fig. 2. The runtime manager constantly assimilates the state of the system including but not limited to channel activity, application mode, and energy availability and decides whether reconfiguration should or should not be done. The procedure of reconfiguration is based on decision-execution sequence. In the first step, the runtime manager uses the selection of the suitable feature module depending on the current system needs. Then part of a bitstream that represents the chosen module is loaded into the reconfigurable portion as the fixed region keeps receiving and buffering incoming information. After reconfiguration, the data processing is immediately resumed using the loaded new module. The method provides uninterrupted availability of the system and reduces the reconfiguration cost.

Flow TZ Flowchart of the partial reconfiguration process at runtime and system monitoring, reconfiguration decision-making, data buffering in the proposed reconfiguring process, and easy resumption of the feature extraction in the proposed FPGA-based architecture.

Channel Scalability and Resource Management

In order to facilitate scalable processing on multiple channels, the architecture uses feature extraction modules that use parameterized datapaths and time-multiplexed computation. Where N is the number of channels that are active. The degree of time multiplexing is adjusted to deal with the effective processing throughput T.

$$T = \frac{f_{clk}}{N} \quad (2)$$

where f_{clk} is the system clock frequency. Runtime adaption enables the programme to compromise the throughput and the consumption of resources as the number of channels changes. Bacterial populations that have less channels being used are re-used more efficiently, and lead to reduced idle logic and power dissipation. The number of channels in a system is dynamically reallocated to fit a real-time processing constraint.

Implementation and Experimental Setup

Hardware Platform

The proposed dynamically reconfigurable feature extraction architecture was inculcated on a Xilinx FPGA based platform that provides dynamic partial reconfiguration (DPR). The FPGA board was set-up through a system-on-chip (SoC) designing flow, where the permanent and reconfigurable areas were established with vendor-supported DPR designing approaches. The sensor data interfaces, input

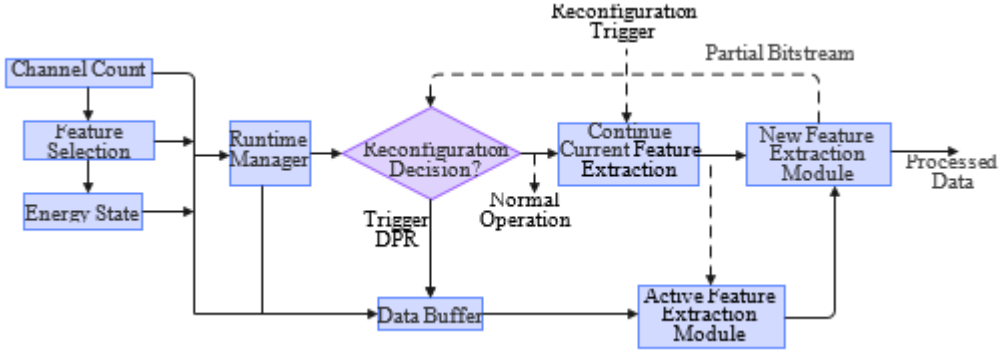

Fig. 2: Runtime Partial Reconfiguration Workflow for Adaptive Feature Extraction

buffering, control logic and the runtime reconfiguration manager are provided in the static region with the feature extractors being provided in the reconfigurable portion. In order to realise the efficient use of hardware and power saving, all the signal processing operations were based on fixed point arithmetic. The word lengths were chosen such that there was a balance of accuracy of numbers and hardware cost, which assures good features extraction at low logic costs and low dynamic power usage. The synthesis, placement and routing of the design were done by standard FPGA design tools, and partial bitstreams, representing each module of feature extraction, were created to run at runtime.

Evaluation Metrics

In the context of the experimental assessment, the metrics are working on the criteria, which directly indicate the appropriateness of the suggested architecture to the processing of real-time multichannel neurophysiological signals. Processing latency per channel Latency is measured as the time per channel, which is needed to calculate the set of features that have been selected by a single channel between the time of entry of input samples in the process and the availability of the output. This indicator is paramount to determine responsiveness in certain time.

The ability of the system to maintain continuous multichannel streams of data is measured through throughput which is defined as the number of samples that are processed per second. Effects of turnaround reconfiguration on the throughput is also examined so that performance decay during reconfiguration is in acceptable levels.

The usage of FPGA resources is measured in the form of look-up tables (LUTs) and flip-flops (FFs), digital signal processing blocks (DSPs), and block RAMs (BRAMs). This measure is used to draw attention to the efficiency improvements brought about by the fact that the feature extraction modules can be loaded dynamically as opposed to loading all the modules at the same time.

Lastly, post-implementation tools of power analysis are estimated in real representative loads under dynamically consumed power. The measures of power put emphasis on the active processing stages in order to realise the benefits of power in reducing resource activation through dynamic r econfiguration.

Baseline Comparison

To determine objectively the advantages of the proposed method, the experimental outcomes are compared to the baseline static FPGA implementation. The baseline design places all feature extraction modules in line with each other and active independent of application requirements. It is a traditional hardware acceleration model that is used in fixed-function FPGA designs. The proposed dynamically

Table 1: Implementation Parameters of the Proposed FPGA-Based System

Parameter	Value / Description
FPGA platform	Xilinx Zynq-7000 SoC (XC7Z020)
FPGA design tool	Xilinx Vivado Design Suite (Version 2020.2)
Clock frequency	100 MHz
Arithmetic format	Fixed-point (Q15.16)
Supported signal types	EEG, EMG, ECG
Number of channels	8–32 (runtime configurable)
Sampling rate	256 samples/s per channel
Processing window size	256 samples
Feature extraction modules	Time-domain, frequency-domain (FFT), time–frequency (DWT)
Reconfigurable region size	~35% of total FPGA resources
Partial bitstream size	450–600 KB (depending on module)
Reconfiguration time	~10–15 ms
Data buffering strategy	Dual-buffer FIFO in static region
Power estimation method	Post-implementation analysis (Vivado Power Analyzer)

reconfiguring architecture as well as the fixed baseline were simulated using the same FPGA card, clock speed as well as fixed-point accuracy to enable a just comparison. Latency, throughput, resource utilisation, and power consumption differences are hence only associated with the choices of the architectural design unlike implementation artefacts. The presented comparative analysis is a clear insight on the benefits of runtime partial reconfiguration in adaptive and energy efficient neurophysiological signal processing.

Implementation Parameters

To improve reproducibility and to be able to present credentials on the experimental configuration, the most important implementation parameters of the suggested dynamically reconfigurable architecture are outlined in Table 1. These are the parameters which determine the hardware platform, design configuration and reconfiguration at runtime which are used during the whole examination.

Results and Discussion

The obtained results of this experiment indicate that the proposed dynamically reconfigurable architecture of the FPGA performs equally well as the traditional stationary design and is much more efficient in terms of hardware. Table 1 summarises the utilisation of the FPGA resources to the proposed architecture and the existing baseline in the varied configurations of feature extraction. In cases of partially activated feature extraction modules, the proposed method results in the use of significantly less logic and DSPs, 3040 times less in fact, which confirms that runtime partial reconfiguration is a useful approach to do away with idle hardware resources. Fig. 3 used above shows that the proposed architecture is deterministic and has the same low-latency processing as the static design. The overhead associated with the reconfiguration is offset with long-run operation and has no impact with the performance of steady-state processing. This also shows that runtime flexibility is possible without opposing real time constraints, which is essential to multichannel neurophysiological signal processing. The dynamic power consumption is obtained and presented in Fig. 4, thus demonstrating the advantages of the suggested approach. Using a balance between the features extraction modules that are actually needed, the architecture requests the dynamic power consumption of the modules to be reduced by a significant amount as compared to idle power consumption in the static configuration. This enhancement goes directly into the implementation of energy-restricted wearable and portable biomedical systems, whereby sustained operation lifetime is a major need. The overhead because of reconfiguration was measured by estimating the time to load incomplete bitstreams at runtime. Reconfiguration of the network only requires a short time interruption virtually covered by input buffering in the stasis region as demonstrated in Fig. 5. This overhead is insignificant when compared to the total execution time of feature extraction tasks, and this fact justifies the viability of dynamic partial reconfiguration to real-time applications.

Compared to previously documented FPGA-based neurophysiological processing systems, which mainly make use of fixed of course-grained programmable systems, the design offers a better use of resources

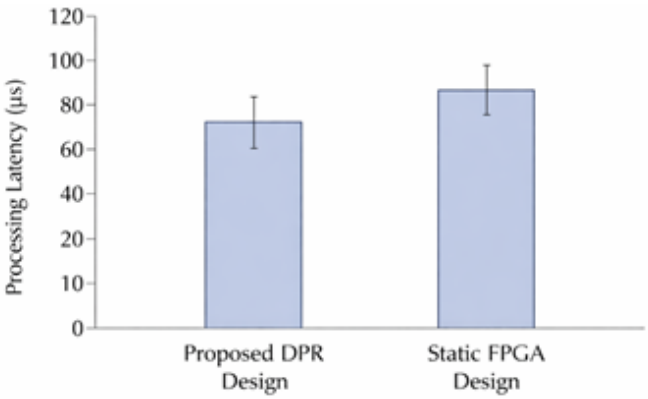

Fig. 3: Processing Latency Comparison Between Dynamically Reconfigurable and Static FPGA Designs

Table 2: FPGA Resource Utilization Comparison Between Static and Dynamically Reconfigurable Architectures

Architecture	Active Feature Set	LUTs (%)	FFs (%)	DSPs (%)	BRAMs (%)
Static FPGA D esign	All feature modules active	68	62	75	58
Proposed DPR Design	Time-domain features only	42	39	28	41
Proposed DPR Design	Frequency-domain features only	47	43	35	44
Proposed DPR Design	Time-frequency features only	50	46	48	47
Proposed DPR Design	Mixed adaptive configuration	44	41	40	43

and power efficiency without diminishing real-time behaviour. These findings indicate that the rich reconfiguraton of a fine-grained runtime can be of significant benefit compared to traditional designs that are static, especially when the counts of channels can be varied and when new features may be demanded.

Comparison between the latency per channel of the proposed dynamically reconfigurable architecture and a fixed FPGA based design.

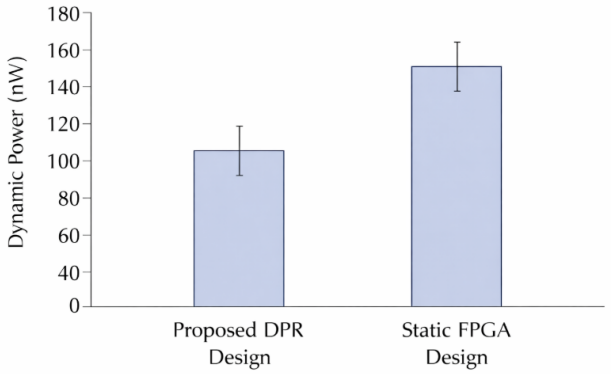

Fig. 4: Dynamic Power Consumption Comparison of Reconfigurable and Static FPGA Architectures

Comparison of Dynamic power consumption of the proposed dynamically reconfigurable architecture, and the static FPGA based design.

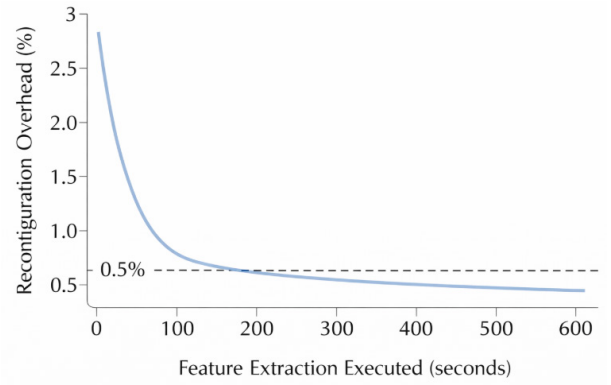

Fig. 5: Reconfiguration Overhead Relative to Feature Extraction Execution Time

Percentage reconfiguration overhead of total execution time of runtime feature extraction under dynamic partial reconfiguration.

Conclusion

The current paper described a dynamically reconfigured FPGA-based hardware design of multichannel neurophysiological feature extraction to solve the issues of scalability, energy efficiency, and adaptiveness of real-time biomedical signal processing systems. The proposed architecture can adapt runtime features extraction functionality to dynamic changes in channel counts, feature requirements and constraints in the system, however, without discontinuing continuous data acquisition or processing by exploiting dynamic partial reconfiguration. The experimental analysis shows that the discussed design has the same processing latency as traditional FPGA implementations that require no dynamic evaluation but uses much less hardware and consumes a lot less dynamic power. The findings substantiate the claim that runtime reconfiguration is an effective practise to erase idle hardware resources and enhance energy efficiency of multichannel neurophysiological applications, most specifically to wearable and embedded systems. The standardised interfaces and modular design taken in this work are facilitating extensibility and reuse and the design will be applicable in a wide variety of neurophysiological monitoring and brain-computer interface applications. The suggested framework will be expanded in the future as the adaptive learning mechanisms designed to automatically optimise the reconfigurating decisions made depending on the signal characteristics and the application context. Other activities will be devoting themselves to hardware prototyping using real sensor data and extending to more neurophysiological modalities, making the proposed strategy even more useful in practise.

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