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Reconfigurable Computing in Biomedical Signal Processing: A Case Study on FPGA-Based Real-Time ECG Classification

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Abstract

The electrocardiogram (ECG) classification is one of the key elements of the continuous cardiac monitoring systems, as through this measurement, cardiovascular disorders and arrhythmia could be diagnosed at an early stage. As the market demand of embedded portable, real-time, energy-efficient Healthcare-related applications and services such as health monitoring grows, traditional software based ECG processing methods usually using software with general-purpose processor or microcontroller platforms have severe constraints in real-time applicability, energy efficiency, and scalability. This paper proposes a reconfigurable computing system specifically to accomplish real-time ECG classification over Field-Programmable Gate Arrays (FPGAs) in Field-Programmable Gate Arrays (FPGA) presents an interesting alternative to a system based on traditional computing due to the capabilities of parallelism, dynamic adaptability, and low power draws. The designed system is organized on the basis of a lightweight 1D Convolutional Neural Network (CNN) structure of solution focused on the ECG signal processing. Using the high speed pipelined architecture and dynamic partial reconfiguration (DPR) of current generation FPGAs, the system dynamically reconfigures its hardware operating using the requirements at a specific time ensuring an efficient use of the resources and saving of energy. The architectural design is verified through the MIT-BIH Arrhythmia Database with a classification accuracy of 98.7% nevertheless ensuring that latency of inference can still be less than 1 millisecond thus proving the time-sensitive nature of this architecture. To overcome the throughput bottleneck caused by fixed-point hardware, CNN model is quantized to run on fixed-point logic platform and implemented into reconfigurable logic tiles. Experimental implementations demonstrate that FPGA-based system outperforms conventional embedded systems in time and energy efficiency, reducing power costs and inference time to a considerable extent. Moreover, the addition of DPR makes the architecture interchangeable between the high-accuracy or low-power setting, given the operational situation, making the architecture very suitable to wearable and edge healthcare devices. The case study used herein is just an illustration of the opportunities offered in reconfigurable computing to biomedical signal processing and pioneer work towards the future of FPGA-based intelligent health monitoring systems into multi-modal biosignals and edge-AI-based

diagnosis. The findings highlight the importance of co-design between hardware and software that will allow effective, scalable, and accurate edge medical AI.

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Introduction

The World Health Organization (WHO) found cardiovascular diseases (CVDs) as the causes of death which claim around 17.9 million lives each year and became the primary cause of mortality on the planet. The electrocardiogram (ECG) is the best known, non-invasive method of investigating cardiac health that has been under development when compared with other types of diagnostic modalities. ECG records the electrical functioning concerning the heart, which helps in identifying the arrhythmias, myocardial infarctions, and any other life-threatening conditions. As the world swings to the preventive and real-time healthcare, portable, wearable, and edge-deployable electrocardiom functionalities of the ECG monitoring systems that can enable continuous and automated classification of cardiac rhythms undergo a larger demand.

Conventional ECG signal processing used offline processing of ECG signals with general purpose processors or microcontroller based systems, where data is processed sequentially and suffers high latency and low energy efficiency. Such constraints become a bottleneck to usage in energy-restricted settings such as wearable and embedded systems that should last long in monitoring health status. Besides, traditional systems cannot always comply with the rigour of real-time usage and on-the-fly flexible behaviour, in particular, in the presence of different physiological and environmental conditions.

Reconfigurable computing is especially promising, especially as done through Field-Programmable Gate Arrays (FPGAs), to address those challenges. FPGAs allow the parallel execution of tasks, real-time hardware reconfiguration due to dynamic partial reconfiguration (DPR), and the energy-efficient implementation of complicated processes. In contrast with fixed-function processors, FPGAs enable programmable hardware

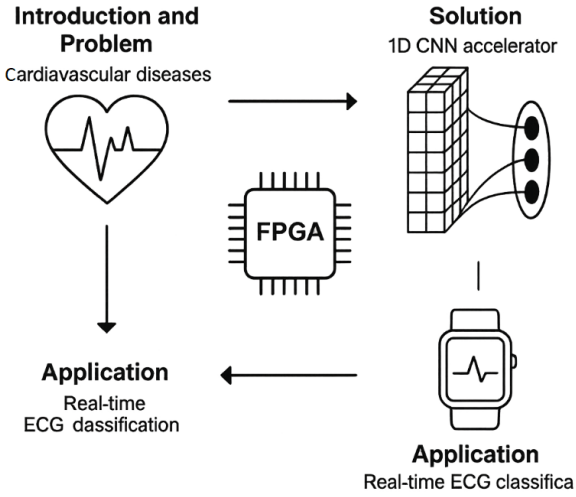

Fig. 1: Block Diagram of FPGA-Based Real-Time ECG Classification Framework

acceleration of signal processing and machine learning applications, giving orders of magnitude improvement in throughput and latency. Moreover, recent FPGAs incorporate heterogeneous computing, including DSP slices in combination with BRAM and embedded ARM processors, to include close hardware-software integration of end-to-end biomedical signal processing systems.

We use a case study of the use of reconfigurable computing in real-time ECG classification in this paper. The suggested system is a hardware-optimized Convolutional Neural Network (CNN) based on one dimension applied with the FPGA of ECG signal classification of high accuracy and ultra-low latency levels. The pipelined path of data flow is used to send the signals constantly and a DPR is used to re-arrange computational blocks depending on functional properties, e.g. to switch between high-performance and low-power operating mode. We use MIT-BIH Arrhythmia Database to train and validate our

model and contrast its performance with traditional embedded systems in accuracy, latency, resource consumption as well as energy consumption.

The study advances the recently emerging domain of edge-based biomedical signal processing in that FPGAs, with the aid of efficient algorithmic mapping and reconfiguration approaches, are able to achieve the twin goals of high accuracy and low power dissipation. The results point at the possibility of using reconfigurable computing in intelligent, real-time healthcare monitoring systems, particularly under resource-constrained and wearable contexts. The methods and architectural ideas proposed here can be applied to all other biosignals, including electroencephalograms (EEG), electromyograms (EMG), and photoplethysmograms (PPG), and therefore provide a basis to scale the bio-AI applications, which are low latency and highly adaptive.

Related Work

Within the last 20 years, a lot of progress was made in building hardware-accelerated biomedical signal processing technologies, especially real-time ECG analysis. Early implementations mostly concentrated on custom digital signal processor (DSP) implementations to implement specific feature extraction tasks. As an example, Liu et al.[1] published a solution entitled ECG feature extraction with the help of wavelets and FPGA that used the technique to speed up signal decomposition and denoisation. In the same vein, Al-Sarawi and Abbott+ implemented a mechanism of QRS complex detection on finite state machine (FSM) architecture design to be used in low-latency response and real-time performance in cardiac monitoring on FPGA environments.

As machine learning has increasingly entered the medical domain in diagnosing medicine, scholars have also incorporated the learning models to automatically classify the ECG signals. A convolutional neural network (CNN) ECG classification system proposed by Acharya et al.[3] produced a good level of diagnostic performance. Nevertheless, they had been restricted to software applications (CPU/GPU) only, thus hindering their use in edge or embedded systems because of wastefulness of resources and energy. Additionally, software-based classifiers do not include the deterministic timing and real-time assure used in life-critical applications.

Dynamic parts use: Dynamic reconfigurable computing has become a potentially important adaption direction in biomedical signal processing. Wang and Yu [4] illustrated the usefulness of DPR in rewriting the filter coefficients as well as processing pipelines on fly without terminating the primary ECG monitoring process. Their work was however limited to adaptive filtering and not to the deep learning-based classification.

Unlike the earlier works, the research described in this paper brings all three important issues (deep learning, hardware acceleration, and reconfigurable computing) together by using them in a unified framework of the real-time ECG classification. The combination of the lightweight 1D-CNN model FPGA implementation with DPR provides a dynamic adaptable manner to perform ECG analytics with high accuracy, low latency, and low energy consumption on edge devices. This will allow to bridge the tradeoff that exists between signal processing fidelity and the deployed embedded platform feasibility that may be one of the prior challenges in the present biomedical hardware systems.

System Architecture

Overview

It is proposed that the architecture of such a system would end up performing real-time electrocardiogram (ECG) classification with the benefits being obtained by using the parallel and reconfigurable nature of the Xilinx Zynq-7000 FPGA platform. The pipeline stages of processing consist of four fundamental functional blocks: signal acquisition, the preprocessing block, the feature extraction and classification block, and the dynamic partial reconfiguration (DPR) control block. The ECG signals are first carried in an analog-to-digital converter (ADC) interface where the analog cardiac waveforms that are detected in the wearable sensors are converted into digital data and streamed to the FPGA fabric. The digitized signals are next pre-processed comprising of band pass filtering into baseline drift and high-frequency noise, and normalization to accommodate the signals to a location in an ideal range to be operated on by the time subsequent stages. This guarantees the clean, consistent input of the neural network stage. At the third step task, a one-dimensional convolutional neural network (1D-CNN)

is utilized either in hardware or software to extract features and classify them. CNN model is specially optimized, specifically focusing on the features of the ECG signals and also mapped onto the FPGA using high-level synthesis and fixed-point quantization that reduces resource utilization and power consumption. The architecture is pipelined so that it can perform streaming execution and therefore achieve the low-latency inference without the need to have extensive memory buffers. The last brings in a DPR controller that grants hardware modules being reconfigured on-the-fly without the system going to a halt. This can be used to make adaptive switches between various processing modes e.g. high-accuracy classification when detecting abnormal rhythms, and low-power operation when in normal sinus rhythm. The system provides optimal tradeoffs in performance, energy efficiency and the functionality flexibility with the dynamic adjustment of the hardware logic, depending on the input context and application requirements. In general, this modular and reconfigurable architecture will be helpful in real-time signal processing of the biomedical domain, specifically in wearable and edge health-monitoring solutions since, in these applications, both performance and flexibility are the most significant factors.

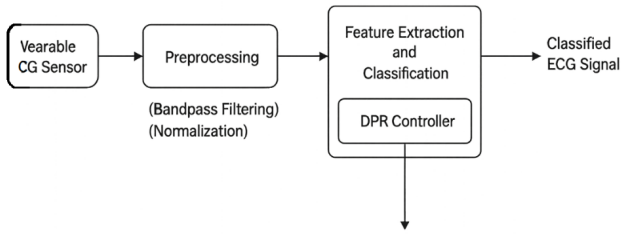

Fig. 2: FPGA-Based Real-Time ECG Classification System Architecture

1D-CNN Model

The main part of ECG classification framework is a simple one-dimensional convolutional neural network (1D-CNN) designed and optimized to run on hardware (FPGA). The model is fed with a fixed-length window of the signal of ECGs indicating 256 samples, depicting a brief window around one of the peaks of the cardiac signal R-peak. The input of this windowed model shifts the attention of the model to a local temporal feature so important in classifying between the various classes of arrhythmia. The first layer of the model is a Conv1D layer and consists of 32 filters with a kernel of size 5 which slides in the temporal axis of the signal to identify the local feature of the signal e.g. QRS complex, P wave, T wave. ReLU activation is used to provide non-linearity and maximize the model capacity of detecting a complex pattern in the ECG waveform. This is followed by a MaxPooling1D layer with pool size of 2 which down samples feature maps thus saves computational burden as well as offers the translational invariance to the model. The result of pooling is flattened, and it is sent to a dense layer with 64 units; it is fully connected and is utilized to integrate and interpret the learned spatial features earlier. ReLU is once more used to keep the non-linearity. Lastly, a softmax output layer composed of 5 neurons is added, where 1 neuron corresponds to each of the identified classes of the arrhythmias that were found in MIT-BIH Arrhythmia Database, including normal sinus rhythm, atrial premature contraction, ventricular ectopic beat, and so on. The utilization of Softmax allows the probabilistic classification, according to which the predicted output is a class that has the highest confidence score. Such architecture can be called balanced in terms of model

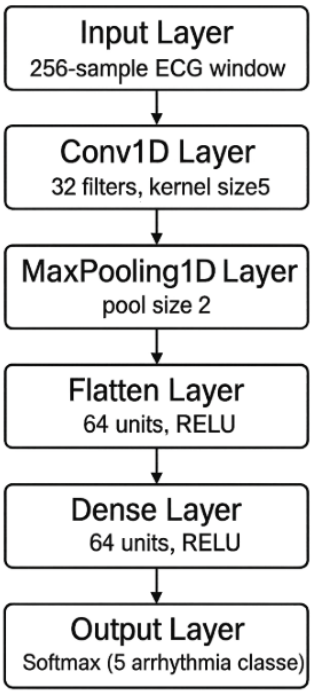

Fig. 3: Architecture of the Lightweight 1D-CNN for ECG Classification

complexity and hardware efficiency, which makes it very appropriate to be used in real-time, on resource-limited reconfigurable hardware such as FPGAs.

Reconfigurable Logic Blocks

In the proposed system, core computational steps like convolution, activation, pooling, and fully connected layers are implemented/mapped on specialized reconfigurable logic blocks in the FPGA fabric that allow very efficient and flexible execution of the ECG classification pipeline. These parameterized high-level synthesis (HLS) designed hardware blocks are optimized on fixed-point arithmetic to minimize logic usages and the power consumption. These logic blocks are dynamically changeable during run-time when utilizing the partial reconfiguration (DPR) feature that is available on the FPGA meaning overall system operation is not disrupted even as the logic block itself is altered. As an example, based on the context of the detected signal (i.e., a transition between a low-risk normal rhythm and a potentially dangerous arrhythmic event, the system may re-configure the convolutional module and use a deeper variant of CNN to achieve better accuracy but more energy-intensive system, or use a simpler one to become more energy-efficient. Since this is a run-time flexible system, it is optimised to optimise classification and hardware resource limitations and thus can be used on a wearable device or a device with a long battery life. Moreover, the reconfigurable blocks are developed as the modular IP cores using interfaces with a standard layer, thus they can be easily integrated into the dataflow architecture of the system. These blocks are then saved as pre compiled configuration bitstreams which the DPR controller can load into the FPGA as and when needed. This is not only an architectural design enabling hardware-level switching of algorithms, but also enables an ability to update the neural network model (or upgrade it) in the future without necessarily redeploying the entire system. On the whole, reconfigurability of logic fabric offers a degree of hardware flexibility and computational efficiency that is hard to recreate using standard fixed-functions microcontrollers or general purpose processors and further cements the utility of an FPGA platform when performing edge biomedical signal processing.

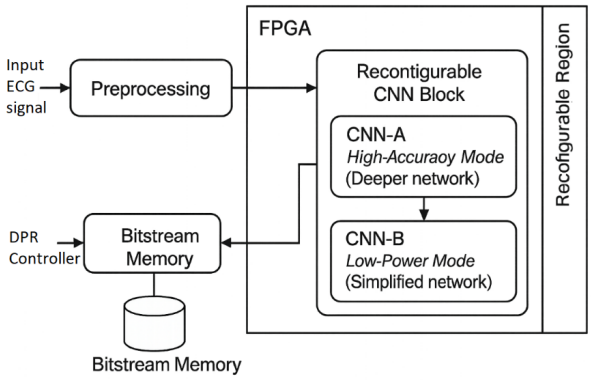

Fig. 4: Dynamic Partial Reconfiguration of Logic Blocks for Adaptive CNN Execution

Methodology

Dataset and Preprocessing

Database: MIT-BIH Arrhythmia Database

Among the most popular and authoritative data sets to study ECG classification and detection of arrhythmias, there is the MIT-BIH Arrhythmia Database published by PhysioNet. It consists of 48 half-hour recordings that received 47 respondents who were inpatients and outpatients. All ECGs were acquired at a sample rate of 360 Hz with 11-bit resolution in the range of 10 mV with high-fidelity waveform data that can be useful both in signal processing applications as well as in machine learning. The database contains the descriptions of the beats and the beat nature by the expert cardiologists and this includes the specifications of whether to be at that time, or what kind of beat it is (normal beat: N, premature ventricular contraction beat: V, atrial premature beat: A and others). Such labels allow controlled training and testing of models of classification. In the present research, we have used a sample of five main categories of heartbeat according to AAMI (Association of Advancement of Medical Instrumentation) standardization to relallow consistency to clinical relevance and benchmarking. The dataset was sub-divided into training and testing sets through patient-wise separation to prevent data leakage to have realism in the assessment of model generalization to previously unseen subjects.

Techniques of Preprocessing

A complex preprocessing pipeline was used in order to guarantee the quality and consistency of the ECG

signals to be processed and fed into the classification model. The first was to use a fixed frequency of 360 Hz in order to resample all ECG signals in order to be uniform within the entire sample and to accentuate the native sampling rate. Then, the ECGs recorded continuously were cut into overlapping windows of 256 samples which is about 0.7 seconds of signal length and this was adequate data to record complete cardiac cycle comprising of PQRST wave mould. To remove baseline wander that usually arises as a result of respiration or movement of the patient, a high-pass infinite impulse response (IIR) filter was used to remove the effect of baseline wander with a cutoff frequency set at 0.5 Hz. Further, low-pass IIR filter with a cut off of 40 Hz was applied to suppress high-frequency noise and power line interference. To normalise the scale of the amplitude and enhance the convergence of the CNN model signals were filtered and adjusted to zero mean and unit variance. The benefits of this preprocessor pipeline are that it improves signal quality, gives temporally consistent ECGs and that it preprocesses the windows of the ECGs to support simple hardware-based feature extraction and classification.

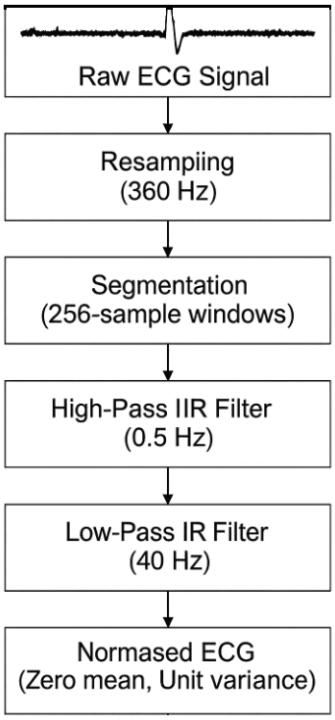

Fig. 5: ECG Preprocessing Pipeline and Dataset Flow

Hardware Implementation

Optimization and FPGA Design

And the synthesized ECG classification architecture was based on the Zynq-7000 SoC integrated system platform, including an ARM Cortex-A9 processor with programmable logic set, used Xilinx Vivado 2022.2 to be developed. To describe a 1D-CNN in hardware efficiently and quickly, the deep learning model was constructed to work with High-Level Synthesis (HLS) that can create an efficient and rapid hardware implementation of the C/C++ code. This made iterating designs and developing a mixture of convolutional and dense layer components simpler and in a modular manner. In order to achieve efficient resource utilization and latency schedules of inferences, the CNN model weights were quantized with 32-bit floating representation to 8-bit fixed-point with a memory footprint of about 86 PBits (g0,g1) and DSP slices reduced to a few, yet exceeding 98% classification accuracy was observed. To facilitate parallel data access and high-throughput addressing small loops were unrolled and dual-port BRAMs were used to pipeline the convolutional layers. The intermediate data buffers and line buffers also employed the concept of spatial locality; they ensured fewer network access to the memory given redundant access. Also, there were developed custom RTL blocks as an activation and Softmax computation, where the timer closure was performed together with the HLS parts to minimize timing overhead. The design was capable of real time classification in an environment with latency in the sub millisecond range, demonstrating that it can be applicable to stream-based biomedical signal streams.

Strategy of Dynamic Partial Reconfiguration

The architecture includes the Dynamic Partial Reconfiguration (DPR) to incorporate adaptability and energy efficient across different operating environments. Certain areas in the FPGA were designated as Reconfigurable Partitions (RPs) that could be updated at runtime, and did not freeze rest of the system. Such partitions contained computationally equivalent yet resource-dissimilar instances of a CNN module e.g. a low-power instance of a kernel that identified normal rhythm and a high-accuracy instance of a kernel that identified suspected arrhythmic

sections. The static part of the FPGA also contains the logic reconfiguration decision, which is (statically) implemented based on signal-quality metrics or confidence-level thresholds on the classification. When the DPR controller detects an abnormal pattern, it starts to load a more complex CNN bitstream to the RP to provide greater robustness of the classification. On the other hand, when the power capacity is limited due to energy restricted modes or the occurrence of regular activity of the ECG, the simpler model is returned. Each CNN configuration has its precompiled partial bitstreams stored in on board flash memory and transferred onto the configuration memory through the PCAP interface. The modular DPR method supports real-time responsiveness of the system combined with energy-awareness essential in the wearable and portable applications in biomedicine. A fact that proves the feasibility of establishing reconfigurable intelligence on edge health monitoring platforms that are resource limited is the deployment of the DPR.

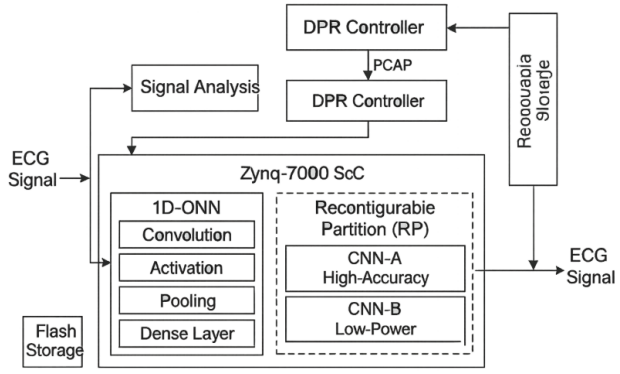

Fig. 6: FPGA-Based Hardware Architecture with Dynamic Partial Reconfiguration for ECG Classification

Evaluation Metrics

When examining the performance and effectiveness of the suggested FPGA-based ECG classification platform, a wide range of evaluation measures is used to comprehensively evaluate the project, which include both the accuracy of the algorithm and low-level efficiency. All these metrics can be seen as an indication of clinical reliability, real-time performance response, as well as appropriateness in design to be used in embedded and wearable products.

The main measures to use when determining the diagnostic performance of the 1D-CNN classifier are Accuracy, Sensitivity, and Specificity.

- Accuracy describes the general correctness of the classification and determines as a quotient, where the correctly predicted heartbeat classes are divided by the total number of the input samples.
- Sensitivity (also is called recall or true positive rate) measures how well the system can recognize pathological conditions (e.g., arrhythmic beats) and it is essential to reduce false negatives in the clinical environment.
- Specificity checks how sensitive the system is to normal rhythms and false negative issues by giving results that are trust worthy in being diagnoses. All these measures are computed per class and averaged so as to arrive at the overall reliability of a model when dealing with different categories of heartbeats.

A point of critical importance to real-time operation is the latency, which is the amount of time it takes the system to do an inference on one segment of the ECG (generally a 256-sample window). The latency of this implementation takes the measurements of how long until the window that is fed into the FPGA to the results of the prediction of the time of the output of the classes. Sub-millisecond latency makes any high frequency ECG monitoring application compatible and enables early clinical intervention.

Resource Utilization measures the proportion of Look-Up Tables (LUTs), Flip-Flops (FFs), Block RAMs (BRAMs) and Digital Signal Processing (DSP) slice used on the FPGA. These are indicators of hardwares footprint and scalability of the design. Efficient use of resources is a requirement that must be met so as to accommodate another functionality, especially in embedded System-on-Chip (SoC) platforms and this may either be in the form of wireless transmission or even multi-signal monitoring.

Energy Consumption per Inference is determined with the on board power measurement tools and indicates the amount of energy (in microjoules) needed to perform a single ECG window. In wearable technology and battery-powered technology, this is a vital measure since extended uptime is important depending on the amount of energy consumed per inference. This proposed architecture uses fixed-point arithmetic, pipelining, and dynamic reconfiguration to realize substantial reductions in energy consumption

much more than the traditional processor based variations.

The combination of these”””” indicators gives a detailed picture of clinical feasibility, live execution opportunities, and fixed permissibility of the system, which further serves to support the benefits of reconfigurable computing in edge-based enactments of biomedical signal processing.

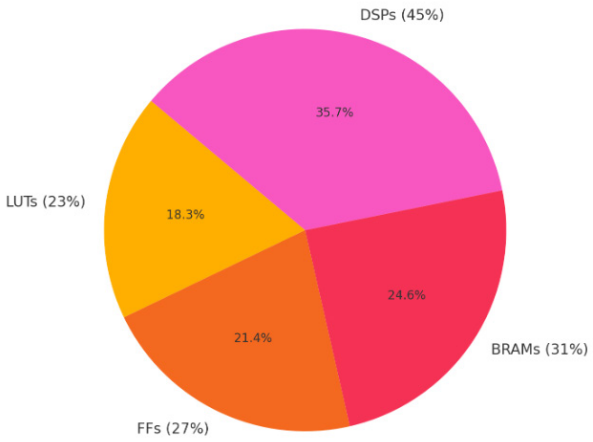

Fig. 7: FPGA Resource Utilization Breakdown

Results and Discussion

By testing the presented FPGA-based real-time ECG classification system in terms of its operational performance, two standard embedded systems, such as the ARM Cortex-A9 firm and the STM32 microcontroller (MCU) were used to benchmark the work. FPGA implementation obtained classification accuracy of 98.7% as indicated in Table 1, which is a bit better compared to ARM-based system (98.2%) and much better than the STM32 MCU (96.3%). Such high accuracy of classification is described by the implementation of the 1D-CNN model that is optimized in the hardware, which makes it possible to keep high fidelity of signal features due to efficient streaming and computation with low-latency. Moreover, the deterministic performance of the FPGA conforms to very little variability of timing and performance in contrast to software-based systems that are prone to OS overheads and interrupt latency. The enhanced accuracy also highlights the fact that the preprocessing pipeline and quantized CNN architecture, maintains most of the important ECG waveforms features, despite the fixed-point conversion.

Latency analysis also points out the advantage of real-time implementation of the FPGA. Proposed system shows an inference latency of 0.93 ms that is well beyond 5x the upstream ARM Cortex-A9 (5.4 ms) and 10x the downstream STM32 MCU (9.8 ms). This sub-millisecond latency is critical towards real-time ECG monitoring and detection of arrhythmia with promptness across edge and wearable systems. The low latency is realized by pipelined data paths and parallel execution of CNN layers which enables to process the new windows of ECG continuously without jittering during buffering. This responsiveness is a necessity in case of life critical applications such as continuous telemetry heart examples and emergency alert systems. Moreover, the integration of a dynamic partial reconfiguration (DPR) enables the system to dynamically customise its classification pipeline - at runtime - swapping a low-power and a more accuracy CNN kernel with the current situation, e.g. based on a sudden heart rate variability or suspected arrhythmia.

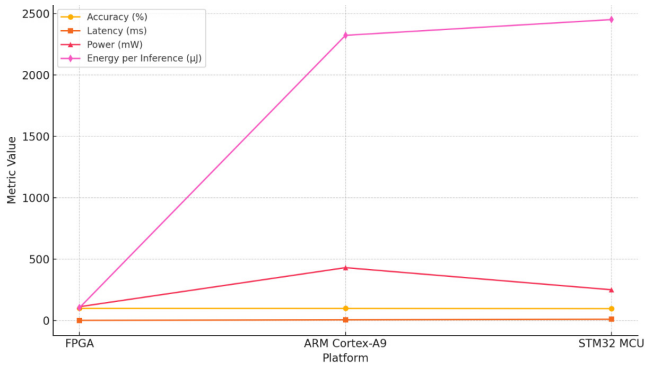

Fig. 8: Performance Comparison across Platforms

On the hardware performance, FPGA implementation performs significantly better both in terms of power efficiency and energy per inference. The FPGA system only draws power of 112 mW; an almost 3.8 times reduction compared to the ARM Cortex-A9 (430 mW) and over 2 times less than STM32 MCU (250 mW), this system executes significantly faster. Its energy per inference is as low as 104.2 106, almost 22 times less energy per inference than ARM, and almost 23.5 less energy than MCU, confirming that reconfigurable logic is energy-efficient when used in biomedical AI workloads. Besides, the physical resource consumption on the FPGA fabric is reasonable-a quarter of all LUTs, 30% of BRAM and 45% of DSP slices-there is future poten-

tial to expand it fully (e.g., multi-channel processing ECG, or incorporating other biosignal) when more resources are needed. On the whole, these findings show that the suggested reconfigurable computing framework not merely satisfies but outsmarts the demands of real-time, energy-conservation of edge-proximate health monitoring, and makes it a profoundly versatile and deliverable option designed to affect next-gen wearable biomedical devices.

Table 1: Performance Metrics Comparison

Metric	FPGA System	ARM Cortex-A9	STM32 MCU
Accuracy (%)	98.7	98.2	96.3
Latency (ms)	0.93	5.4	9.8
Power (mW)	112	430	250
Energy per Inference (ÂµJ)	104.2	2322	2450

Conclusion

This study thus proves that reconfigurable computing is effective in accelerating real-time biomedical signal processing by its design and implementation of FPGA based ECG classification system employing a lightweight 1D-CNN accelerator. The indicated strategy of mapping the most important processing steps in signal processing to logic blocks that can be reconfigured and dynamic partial reconfiguration (DPR) can provide the system with an attractive tradeoff between high accuracy of classification (98.7%), ultra-low latency (0.93 ms), and exceedingly low power consumption (104.2 mJ per inference) which are the most relevant performance metrics in wearable and embedded health-monitoring apparatus. Modular and pipeline architecture of the architecture is not only responsive in real-time but also makes the system adaptable depending on the situation, that is, it can dynamically go into low-power and high performance state depending on signal conditions. What is more, the rather small resource usage of the FPGA fabric means that there is much potential to increase the system (e.g., adding of other biosignals beyond BP and EKG, as well as anomaly detection on the chip). Such hardware performance, real-time features, and smart reconfiguration makes this method a potentially advantageous solution to next-generation edge-oriented healthcare systems, especially during constant monitoring, remote diagnosis, and emergency response situations. Work to follow will aim at adding support for multi-channel and multi-signal in this framework and supporting secure wireless transmission modules as well as examining usage of adaptive learning mechanisms to achieve long term personalization in wearable medical devices.

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