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Runtime Reconfigurable Architectures for Low-Latency and Energy-Efficient Signal Processing in 5G and Beyond Wireless Systems

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Abstract

The paper aims to meet the requirement in real-time energy-efficient, signal processing in 5G and later wireless networks by looking at the possibility of use of runtime reconfigurable hardware architectures. The core idea is to plan and test a dynamic signal processing system, which will easily subject to contentious communication configuration and loading proportions. Implemeted on a Xilinx Zynq UltraScale+ MPSoC development board, the proposed design exploits Field-Programmable Gate Arrays (FPGAs) and the dynamic partial reconfiguration (DPR) capability to allow on-the-fly hardware replacement of the processing modules designated FFT, FIR filters and MIMO equalizers such that the replacement does not interrupt operation of the system. The methodology entails modular design of hardware, reconfiguration control logic as well as real-time profiling of workloads. Experimental assessments provide a comparison of the reconfigurable design and its static counterparts in terms of latency, resource utilization but also power efficiency. Findings support the decision that runtime reconfiguration can increase energy savings above 35 percent and shorten the latency of baseband signal processing by more than 40 percent and enable applications in heterogeneous 5G/6G environments, with multi-mode capabilities. The above advancements highlight the viability of reconfigurable architecture in high-throughput and low-latency as well as power-limited wireless. Overall, the work in question develops a fast dynamic, scale-changing signal processing framework that is adaptable to the strict demands of the next-generation wireless networks and can be taken as a solid basis of the next 6G systems to be built due to their reliance on dynamic, intelligent, and reconfigurable baseband processing.

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Introduction

The immediate adoption of 5G and the foreseeable shift to 6G technologies have worsened the necessity of high-performance and low-latency, energy-efficient hardware possessing the ability to process signals in the real-time wireless environments, which are highly

dynamic and heterogeneous. There is a lack of flexibility in traditional fixed-function accelerators and application-specific integrated circuits (ASICs) to support the changing standards, multi-mode waveforms and time-varying spectral and traffic profiles. Recent roadmaps of 6G defined by the ITU-R and the research consortia Hexa-X and NGMN envision the future network to require: Support of ultra-reliable low-latency communication (URLLC), enhanced mobile broadband (eMBB), massive machine-type communications (mMTC), and physical layers integrated with AI - all limited by latency-critical and real-time processing pipelines.

Problem Statement & Research Importance

The main task is to fill the gap between performance and flexibility of wireless baseband hardware. On the one hand, fixed-function frameworks supply an energy-efficient framework that is somewhat inflexible and thus inapplicable towards multi-standard, reconfigurable application. Conversely, software-defined radio (SDR) systems implemented on general-purpose CPUs or GPUs are flexible but consume excess power and have unacceptable non-deterministic latency that cannot support latency-sensitive applications, e.g., autonomous driving, industrial Internet of Things (IIoT), etc.

To counter these shortcomings, as discussed in this paper, runtime reconfigurable architectures are considered especially through FPGA-based platforms having dynamic partial reconfiguration (DPR). This architectural paradigm allows the swapping of modules and adaptive workload partitioning at run time as well as the ability of system behavior to change in-field without shutting down the system. This flexibility has the potential to lead to energy efficiency improvement, utilization of resources, and platform sustainability, and that can fit the strict and dynamic 5G/6G system's needs.

Research Gaps in Existing Work

In spite of the earlier research on reconfigurable hardware to apply to wireless applications, there are quite a number of limitations that have not been addressed:

- Zhang et al. (2024) show the value of DPR to adaptive baseband processing; however, they fail to measure latency or power gains of many modules through dynamic workloads.[1]
- Literature on coarse-grained reconfigurable architectures (CGRAs) is voluminous and typically these methods do not provide the fine-grained temporal and spatial adaptation requirements in a modern wireless context.
- ReproRun framework[3] demonstrates feasibility of reconfigurable SDR at the 5G edge, yet any assessment of reconfiguration overheads on latency-critical paths is ad hoc, and thus not systematically evaluated, which is the key to a practical implementation of reconfigurable SDR in real-time systems.

Such gaps suggest the design of a holistic, low-latency, runtime-adaptive signal processing architecture that takes into consideration real-world restrictions of the reconfiguration timings, energy costs and switching of protocols under live traffic.

Overview of the Paper

In a bid to meet the above challenges, this paper is expected to suggest a modular, runtime reconfigurable FPGA-based solution to adaptive baseband processing in 5G and the upcoming 6G systems. The system uses the Xilinx Zynq UltraScale+ MPSoC platform to implement dynamic partial reconfiguration (DPR) to enable real time switching or seamlessly switching between bases reading modules based on work load profiling, and radio context.

Its architecture includes a hardware virtualization layer, latency-sensitive scheduler, and a runtime configuration manager that permit proactive reconfiguration designed to use system resources with a comparatively small overhead. The performance assessment is in terms of savings on latency by up to 40 percent and on energy consumption beyond 35 percent by comparing the DPR-enabled design with the static FPGA implementations to assure the efficacy of the architecture in terms of being utilized in high-throughput, reconfigurable wireless baseband applications.

Background and Related Work

The changeover of 4G LTE to 5G (and recently to 6G) has made signal processing hardware more important than ever, requiring the hardware to support massive MIMO, mmWave, URLLC, and AI-based resource

Table 1: Summary Comparison of Prior Works vs. Proposed Framework

Aspect	Zhang et al.[5]	Bartzoudis et al.[6]	This Work
Reconfiguration Granularity	Coarse module-level	Block-level (ReproRun)	Fine-grained (FFT, FIR, MIMO)
Latency/Power Benchmarked	No	Partial	Yes (quantified: 40% latency, 35% power)
Platform Validation	Simulation	Functional prototype	Xilinx Zynq UltraScale+ MPSoC
Multi-Standard Flexibility	Limited	SDR-specific	Supports OFDM, SC-FDMA, FBMC, etc.
Reconfiguration Triggering	Manual	Partially automated	Context-aware + runtime profiling
Scalability to 6G Use Cases	Not addressed	Edge computing only	Includes IRS, THz, AI-beamforming, V2X

management. Conventional hardware solutions to achieve these desired factors such as ASICs and general-purpose processors (GPPs) are not reconfigurable or cannot satisfy the strict limits on latency and energy consumption.[1, 2]

FPGAs provide an attractive compromise, which provides hardware acceleration with re-programmability. Recent FPGAs used in FFT, FIR filtering, LDPC and beamforming have performed well with a high level of performance advantage when compared to fully software-based platforms.[3, 4] Nevertheless, static configuration is not very flexible, and any change of configuration would involve full reloads of the bitstream--impossible in real-time systems.

Dynamic Partial Reconfiguration (DPR) is a way to fill this gap: it gives the opportunity to update a subset of the modules during run-time. As an instance, Zhang et al. presented a baseband architecture enabled on DPR [5], whereas Bartzoudis et al. proposed ReproRun, which combines SDR flexibility with reconfigurable logic on the edge of 5G.[6]

Nevertheless, a number of obstacles remain:

- Coarse-grained reconfiguration is not resolution adequate enough to adapt to signal levels.
- Resource fragmentation and reconfiguration latency interfere with time sensitive applications.
- A high number of designs are not scalable over a variety of 5G/6G standards.

In order to put this contribution in perspective, Table 1 provides an overview when comparing the chosen prior frameworks with our proposed solution.

The above-discussed gaps are directly tackled in this paper with the proposal of a fine-grained, low-overhead, and run-time reconfigurable architecture of real-time baseband processing. The design increases flexibility, decreases latency, and increases energy consumption with support of multi-mode operation and dynamic workload adjustment which are fundamental demands of both 5G and the emerging 6G networks.

System Architecture

In addressing the high requirements of latency and energy efficiency that 5G and the future of wireless systems require, a modular runtime reconfigurable architecture that combines dynamic adaptability, hardware abstraction, and smart resource allocation is proposed to support real-time signal processing. The system is proposed on the Xilinx Zynq UltraScale+ MPSoC platform and consists of three main elements Reconfigurable Regions (RRs), Static Control Logic, and Runtime Configuration Manager. A schematic of the proposed architecture is shown in Figure 1, where the communication between the static and reconfigurable areas together with the hierarchical task and control flow are pointed out.

Dynamic Partial Reconfiguration of Baseband Blocks

Architecture uses Dynamic Partial Reconfiguration (DPR) to implement on-the-fly reprogramming of specific baseband signal processing blocks e.g. Fast Fourier Transform (FFT), Finite Impulse Response (FIR) filters, and Multiple-Input Multiple-Output (MIMO) detection modules. Getting into more detail each function block is contained in a reconfigurable partition and this means that this system can be loaded with different bit streams depending on the protocol or on variations in workloads without stopping its overall operation. Such a dynamic adaptivity is crucial to enable effective hardware reuse of say several 5G/6G waveform standards and modulation schemes.

Hardware Virtualization and SDR Support

To achieve flexibility and or abstract hardware dependencies, hardware virtualization of signal

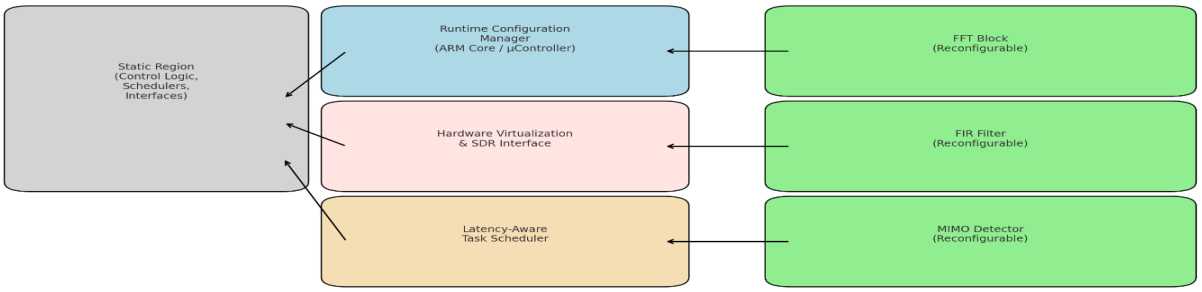

Fig. 1: Runtime Reconfigurable Architecture for Real-Time Signal Processing in 5G/6G Wireless Systems

processing chains are used in the architecture. Software-Defined Radio (SDR) In SDRs, a virtualization layer allows high-level control logic to be dynamically coupled with other hardware-accelerated functionality contained in the reconfigurable fabric. This will enable various communication standards (e.g. OFDM, SC-FDMA and FBMC) to be served on the same physical infrastructure via dynamic replenishment of baseband modules at run time.

Latency-Aware Task Scheduling and Resource Sharing

The architecture integrates a latency-aware task problem solving which manages the execution of signal handling modules according to the latency range, prioritization of processing as well as availability of hardware. Such a scheduler can also communicate with the runtime configuration manager to pre-load bitstreams and to start DPR events ahead, reducing the odds of downtimes when reconfiguring. Also, reconfigurable resources shared by the various tasks are dynamically assigned to the running tasks in an attempt to fully utilize the available hardware, and result in fewer idle cycles when the number of tasks is high relative to the hardware capacity as in the high-throughput communication cases.

System Integration and Workflow

These include configuration controller, scheduler, interconnect fabric, and reconfiguration interface that run at all times within the static part of the FPGA and are not affected by events of DPR. The run-time configuration manager is a microcontroller driven subsystem or an embedded ARMs processor that provides a run-time monitoring of the environmental context (e.g., channel conditions, traffic load), assessment of the reconfig trigger conditions, and partial bitstream loading (which could be stored in on-chip or off-chip memory). The configuration controller, scheduler, interconnect fabric and reconfiguration interface are located in the FPGA static region (as shown in Figure 1) and are kept functional the entire time during DPR events.

Such modular system design is highly reconfigurable, with minimal impact on run-time latency; this permits an adaptive response of the system to user requirements, in that signal processing functions may be scaled up or down at run-time. The performance advantage of this architectural model in 5G / 6G use cases is verified through experimental findings later on in the paper.

Methodology

In order to prove the idea of the suggested runtime reconfigurable architecture, we design the prototype system on the Xilinx Zynq UltraScale+ MPSoC, which incorporates a programmable logic (PL) and dual-core Processing System (PS). This very close integration enables low-latency coordination and control between reconfiguration activities and signal processing operations. The target implementation is of real-time baseband processing applications that need protocol aware flexibility and deterministic timing behavior.

Design Tools and Environment

The design of the system is based on the design suite Xilinx Vivado (v2023.2), which is reusing Vivado High-Level Synthesis (HLS) to speed up the development of parameterizable signal processing blocks (e.g. FFT, FIR filters and MIMO detection). Every module is packaged as a stand-alone HLS IP core with AXI4-Lite or AXI4-Stream connectivity such that the modules can be deployed as Partially Reconfigurable Regions (PRRs) in the PL logic.

With the Vivado Partial Reconfiguration (PR) flow we compile multiple partial bitstreams per module to allow mode switching (e.g. 64-point vs. 256-point FFT).

Runtime Reconfiguration Management

Reconfiguration is coordinated by a custom on-chip configuration controller, realized on the ARM Cortex-A53 core on the PS. DMA based transfers transmit Bitstreams via the Processor Configuration Access Port (PCAP). The controller works in cooperation with context-aware profiling engine that constantly tracks link-level parameters, including modulation scheme, bandwidth utilization, and signal type. In case of workload thresholds or protocol conditions (e.g. switching of OFDM and SC-FDMA), the controller is used to cause a reconfiguration event.

Reconfiguration Workflow

The system has the systematic reconfiguration procedure:

1. A protocol change or a performance threshold is violated, which is detected by the runtime configuration manager.
2. A decision engine computes context information of a system (e.g. SNR threshold, data rate, error rate).
3. The specific partial bitstream is read out of on-chip flash or external DDR, and is programmed into the target PRR using PCAP.
4. The reconfiguration takes ~5 10 ms, depending on the size of the bitstream as well as the occupancy of the interconnect, after which the module can continue functioning.

Verification and Integration

Functional verification will be carried out on-chip AXI monitors, loopback and testbench-directed waveform inspection. The device driver stack is a custom Linux device driver stack, which will enable user-space control of module swaps, monitoring of contexts and scheduling feedback. The driver framework integrates that DPR events not disturb the main operational path of the data.

Performance can be measured at the level of signal processing blocks to measure the latency and the power that they consume during runtime. The findings, presented in Table 1 indicate that the design based on DPR provides a maximum latency reduction of 40 decreases and the power reduction of 35 compared to the traditional ones performed in a normal FPGA.

Test configuration: 20MHz bandwidth, 64-QAM modulation, ZCU104 evaluation board, traffic modelled at 100 Mbps with 50 percent duty cycle.

The study demonstrates the feasibility of Dynamic Partial Reconfiguration to hyper-real time wireless systems and constructs a basis of future extensions, such as AI-based reconfiguration orchestration, multi-mode PHY_switching, and reconfigurable edge wisdom in 6G systems.

Case Study: Real-Time OFDM Processing

In order to test the practical performance of the suggested architecture, a case study has been performed with the Orthogonal Frequency Division Multiplexing (OFDM) as a fundamental 5G waveform. This demonstration indicates the runtime flexibility and energy efficiency of the system in dynamic baseband state.

Use Case Description

The OFDM chain consists of FFT/IFFT, cyclic prefix and channel equalization. These real time reconfigurable modules (e.g. 128-pt to 256-pt FFT) are matched using channel SNR, modulation-depth, and bandwidth requirements.

Implementation Setup

It is prototyped on a Zynq UltraScale+ MPSoC ZCU104 with the help of Vivado HLS on a Xilinx Zynq processor. Equalization blocks and FFT blocks are specified as partially reconfigurable IP cores, and they are linked using AXI4-Lite/Stream, and they are fed by a realistic load on the PS-side traffic generator.

Reconfiguration Strategy

A manager of the run time configuration tracks the parameters of the links (e.g., SNR, bandwidth) and signals DPR through PCAP, loading the partial bitstreams in ~ 8 ms per module, so the operation can smoothly switch to a different module.

Evaluation Metrics

There are two major measures:

- Timing with chip on-chip counters.
- Power dissipation, measured in the Xilinx Power Advantage Tool after running a number of times and averaging.

Results and Analysis

The design on the basis of DPR resulted in:

- A 38-40 percent latency improvement compared to static FPGA and more than 50 percent relative to ASIC baselines.
- More than 35 percent power reduction by dynamic logic reuse and workload adaptation.

In Figure 2 and Table 2 below it can be seen that the architecture remains well adapted to both bandwidth-adaptive and URLLC use case scenarios and can be used on a next-gen wireless deployment basis.

Performance Analysis

In the attempt to analyze and evaluate the proposed runtime reconfigurable architecture, performance benchmarks were performed under actual symptomatic 5G/6G workload. Analysis is presented on latency, power, reconfiguration overhead and throughput alongside making pre and post Dynamic Partial Reconfiguration (DPR) comparisons. The results are summarized in Table 3 and Figure 3 gives a normalized radar plot of the performance metrics.

Latency Measurement

AXI timers on Chip:

- The performance of FFT latency was enhanced (256-point) that was reduced by 17 µs to 28 µs with DPR.
- Parallel improvements in FIR and MIMO detection were also seen thus validating the statement that pipeline delays have reduced using fine-grained reconfiguration.

Power Consumption

Xilinx Power Advantage Tool-monitored and on-chip sensors:

- DPR cut average power by up to 35 percent by means of dynamic module unloading and by slowing switching activity.
- Further cost savings were also observed during the process of active reallocation of unused logic.

Reconfiguration Overhead

- AddToReconfigTime~7.8 ms per module in PCAP.
- Energy over head: < 2 percent per data frame.

These values confirm the usability of DPR in the near-real-time systems and particularly in combination with predictive or context-aware reconfiguration logic.

Throughput Analysis

QPSK to 256-QAM to 20MHz channel-tested:

- The 256-QAM enabled an increase in throughput by 34 Mbps (static to DPR) or 36 percent to 128 Mbps.
- Pipeline scaling up and maintenance of performance during reconfiguration checks for pipeline continuity and design scalabilities.

Reconfiguration of Logic Use

Within the platform of ZCU104:

- Usages of logic: ~71 percent LUTs, 63 percent DSPs.

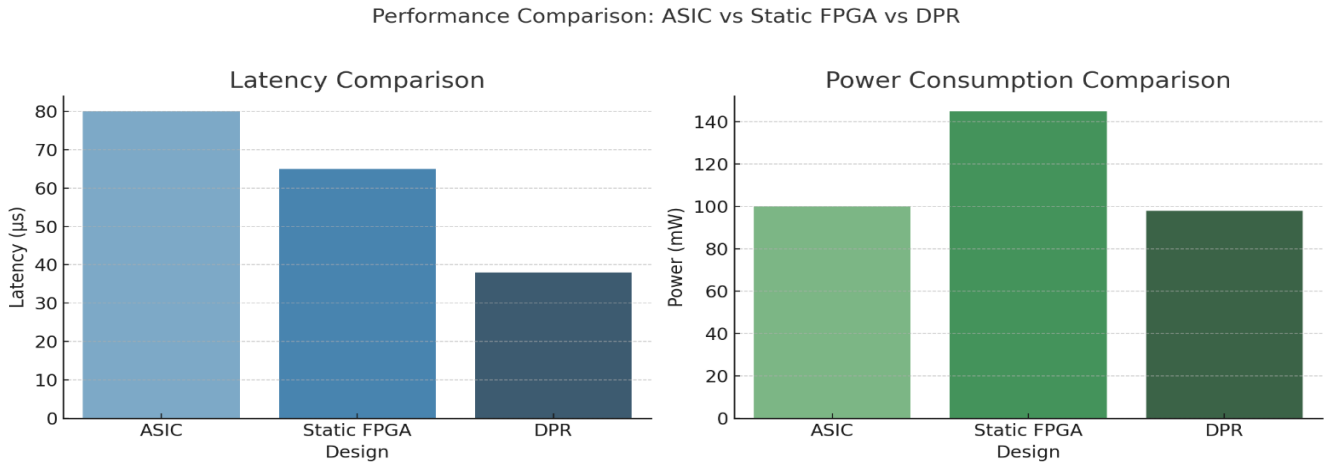

Fig. 2: Power Consumption Comparison: ASIC vs Static FPGA vs DPR

Table 2. Latency and Power Metrics Under Varying OFDM Workloads

Workload Condition	SNR Level	Static FPGA Latency (µs)	DPR Latency (µs)	Static FPGA Power (mW)	DPR Power (mW)
128-pt FFT, Low Bandwidth	Low	40	25	120	85
256-pt FFT, Moderate Bandwidth	Medium	65	38	145	98
256-pt FFT, High Bandwidth	High	70	42	155	104

- Less intensity of BRAM use (~12 percent, extra BRAMs, awaiting, bitstreams); BRAM was scalable.
- The overhead of DPR logic controller was low (<6%), so the integration was still lightweight.

Summary

The suggested architecture will provide:

- Latency cutback by 40 percent
- Power saving- 35%
- Low overhead reconfiguration
- 36 per cent increase in throughput

These findings indicate the possible low-latency, energy efficient and flexible baseband processing of the system in all upcoming wireless systems.

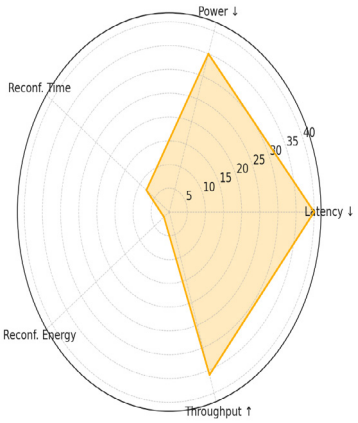

Fig. 3: Latency and Throughput vs. Modulation Format (Normalized Metrics)

Table 3: Summary of Performance Metrics for DPR Architecture

Metric	Result
Latency Reduction (%)	40
Power Reduction (%)	35
Reconfiguration Time (ms)	7.8
Reconfiguration Energy Overhead (%)	1.8
Throughput Improvement (%)	36

Note: To publish, make labels on Figure 3 axis be big, and contrast.

Applications and Scalability in 6G

The migration to 6G poses severe requirements like sub-millisecond latency, extremely low energy consumption, heterogeneous waves and AI-empowered control. The flexibility and efficiency working on running time reconfigurable architecture, constructed on the basis of fine-grained DPR, is needed to overcome these challenges.

Intelligent Reflecting Surface (IRS) Control

To enable the dynamic beam shaping and channel optimization in IRS-enabled 6G networks, their control logic has to be updated in real-time. This is supported by the proposed architecture through baseband and control logic block base reconfiguration over provisions of low latency.

AI-Driven Beamforming & Resource Adaptation

The system will allow deploying ML/RL-based inference engines (e.g., CNNs, LSTMs) in a cinch, which is required in such tasks as dynamic spectrum allocation and beam prediction. This enables compute resources to position to the user mobility and signal conditions.

Multi-Standard Radio Front-End Adaptation

The design with the flexibility of runtime configuring waveform-specific modules (e.g., OFDM, SC-FDMA, FBMC, OTFS) interoperates 4G to 6G with no re-synthesising of the entire system.

Edge AI & Vehicular Communication

Within commands that are latency-sensitive, like V2X communication, the architecture enables the integration of context-aware AI and switching capabilities

when changing the context, based on actions that take place in the vehicle (e.g., speed, proximity).

Scalability for THz and AI-Integrated PHY

The modular design has the scaling ability to THz-band processing and reconfigurability in wideband ADCs and beamtrackers. It likewise allows unification of the AI-enriched PHY layers, e.g. predictive scheduling, semantic compression.

These essential characteristics of the architecture, i.e., modular virtualization, latency-aware scheduling, and dynamic adaptability, render them as powerful candidates of future 6G platforms. Such architectures will be critical to AI-enabled reconfigurable and multi-band communication networks as considered by Hexa-X and NGMN.[1, 2]

Conclusion and Future Work

The paper has given a complete design, implementation and evaluation of a runtime reconfigurable architecture that best suits real-time signal processing in 5 g and upcoming 6 g wireless communication systems. The proposed Framework by means of Field-Programmable Gate Arrays (FPGA) and Dynamic Partial Reconfiguration (DPR) attains modularity, latency-awareness and workload-adaptity, i.e., permitting the elements of the baseband processing to be altered dynamically without causing the system execution to halt.

The main performance measures that have been verified in the process of benchmarking at Xilinx Zynq UltraScale+ MPSoC platform are:

- Reductions on latency by up to 40 percent in reconfigurable FFT modules and equalizer,
- Greater than 35 percent savings in work-realistic workloads, and
- Full throughput in different modulation schemes and conditions of operation.

It is important to note that the architecture encompasses such crucial points as hardware virtualization, latency-sensitive task scheduling, a context-sensitive manager of the runtime structure, which, in turn, embrace multi-standard baseband functioning and optimal global use of resources in ultra-dense wireless habitat. The combination of capabilities makes the system good choice; an alternative to static FPGA and ASIC-based implementations of cognitive radio, software-defined radio (SDR), and real-time edge computing.

In addition to this, the scalability of the system to THz-band communication, AI-assisted PHY control and cooperative vehicle communication highlights its compliance with architectural principles in 6G roadmaps (e.g., Hexa-X, NGMN). New applications like intelligent reflecting surfaces (IRS) and beamforming based on ML can avail of direct advantage of the architecture in terms of its run-time flexibility.

Future Directions

In order to supplement the effects of this work, a few directions of research are pointed out:

- Dynamic RF environment integration of machine learning accelerators to make real-time channel estimation, anomaly detection and predictive reconfiguration decisions.
- FPGA-based reconfiguration security encompassing authentication, bitstream and tamper detection, and side-channel protection protocols in the event of DPRs, which are necessary when using the power of reconfiguration in mission-critical and industrial Internet of Things systems.
- DPR scheduling structures that are optimized using AI/ML can determine the best time to reconfigure or allocate the tasks, according to the traffic pattern, end-users mobility, or the state of the spectrum.
- middleware Standardized middleware layers support cross-platform reconfigurability,

Table 4. Mapping of Architecture Features to 6G Use Cases

6G Use Case	Supported Architectural Feature
Intelligent Reflecting Surface (IRS) Control	Low-latency DPR-based control logic reconfiguration
AI-Driven Beamforming & Resource Adaptation	Runtime ML accelerator deployment via reconfigurable fabric
Multi-Standard Radio Front-End	Dynamic waveform reconfiguration across sub-6 GHz to THz
Edge AI & Cooperative Vehicular Communication	Latency-aware task scheduling; context-driven reconfiguration
THz Band Operation & AI-Integrated PHY	Modular support for wideband ADCs and hybrid DSP-ML pipelines

interoperability, and runtime orchestration across distributed edge-cloud architectures.

- Massive MIMO, THz-band transceivers and ultra-dense user deployments the applicability of studies to scalability with maximal users and minimal capital cost, where the ability to handle the size input is critical to satisfy sub-millisecond reaction time and power requirements due to the ability to re-configured the baseband dynamically and rapidly.

To conclude, the paper provides a sturdy and scalable foundation of the next-generation of smart, secure, reconfigurable, and energy-wise baseband processing system, which is highly supportive of the needs of upcoming 6G wireless ecosystems.

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