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Carbon Nanotube and 2D Material-Enabled Nanoelectronics for Next-Generation High-Performance Circuits

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Abstract

The aggressive scaling of silicon based complementary metaloxide semiconductor (CMOS) technology is also nearing fundamental physical and economic limits, and new materials are being investigated to make next-generation nanoelectronic circuits. Carbon nanotubes (CNTs) and two dimensional (2D) materials, such as graphene, molybdenum disulfide (MoS'(2)), and hexagonal boron nitride (h-BN), have come to be considered transformational candidates due to their superb electrical conductivity, high carrier mobility, excellent thermal management, and flexibility. This paper outlines an extensive literature review and investigation of CNT- and 2D material powered nanoelectronics to be used in high-performance, energy-efficient circuitry. First, the inherent characteristics of such materials, including their manufacturing methodology, and key device level parameters governing circuit performance will be studied. It is discussed also in CNT-based field-effect transistors (CNTFETs), MoS 2 thin-film transistors (TFTs), and hybrid heterostructure devices, in terms of especially scaling behavior, electrostatic control, and integration with interconnects. Comparative simulation and experimental reports suggested that CNTFET-based logic gates could improve energydelay product by up to 3x and reduce static power dissipation by ~40 percent compared to state of the art FinFET nodes, and that MoS 2-based transistors can exhibit ON /OFF ratios greater than 10^6 and subthreshold swings as low as a few times the thermionic limit (~60 mV/dec). Fabrication issues--such as chirality control, wafer-scale transfer, reduction of contact resistance, and compatibility with CMOS-compatible thermal budgets--are also discussed, as well as recent developments in the use of directed self-assembly and low-temperature growth techniques. Lastly, application areas that are potential, which include: ultra-low-energy computing, flexible electronics, terahertz communication, and neuromorphic computer, are identified. With this homework (bridging materials science, device engineering, and circuit design), this paper presents a clear path to making CNTs and 2D materials useful in large-scale, commercially viable nanoelectronic systems.

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Introduction

The semiconductor industry has previously been dependent on an ongoing process of miniaturization of the silicon-based complementary metal oxide semiconductor (CMOS) devices in order to maintain incremental gains in computation performance, energy consumption, and increase in integrations density. This mode of scaling has been behind the historical success behind modern electronics described by Moore law. But at technology nodes beyond the sub-5 nm regime, the technology of traditional silicon CMOS has formidable physical and economic impediments to overcome. The short-channel effects, larger gate leakage as a result of ultra thin oxides, and random dopant fluctuations caused variability which deblackens the device reliability and energy efficiency. Moreover, the rising fabrication complexity of advanced nodes poses a serious threat on the long-term economic feasibility of the traditional scaling due to drastic cost increments of manufacturing.

In consideration to these, researchers are currently investigating alternate channel materials and device structures that are able to provide other gains in performance over time as well as avoiding inherent limitation effects of bulk silicon. Carbon nanotubes (CNTs) and two-dimensional (2D) materials comprise some of the most promising candidates since they have a unique combination of atomic-thickness, exquisite electrical properties and heterogeneous integration compatibility.[1] Carbon nanotubes have a quasi-one-dimensional structure, resulting in near-ballistic carrier transport and allowing high tolerance of current density (>10 9 A/cm 2), and excellent thermal conductivity; they are thus suited to applications in active devices and in interconnects. They have a tunable bandgap governed by chirality and diameter so as to make high performance field-effect transistors (CNTFETs) with sharp subthreshold slopes and small leakage characteristics.[2]

CNT and 2D material platforms will allow many device architectures, including passive devices like inductors, and active devices like FETs, creating nearly seamless integration between high-frequency, low-power, and flexible electronics applications as shown in Figure 1. Two-dimensional materials, including graphene, molybdenum disulfide (MoS2) and hexagonal boron nitride (h-BN) are complementary to CNTs because they support atomically thin channels to offer improved electrostatic control of their gate channel, which mitigates short-channel effects at aggressive scaling lengths. Graphene has ultra-high carrier mobility (>200,000 cm 2 /V s) and unusual mechanical flexibility, which is why it is also suitable in high-frequency and flexible electronics. As an example, transition metal dichalcogenide (TMD), MoS 2 has a large and direct bandgap (~1.8 eV for monolayer), which makes it useful in logic devices, having low off-state leakage and large ON/OFF current ratios. h-BN has a large bandgap and highly insulating characteristics, which make it an excellent substrate material or dielectric layer in van der Waals heterostructures to create highly performing transistors without defects.

Combining CNTs and 2D materials in nanoelectronic system paves the way of achieving circuits working at a high frequency with ultralow power consumption, new form factor, e.g., flexible, wearable and transparent electronics. With the recent gains in synthesis, transfer and integration technologies, it is now possible to make wafer-scale devices of CNT and 2D materials now with increasing yield and uniformity, taking the materials a step closer to large-scale industrial applications. Nonetheless, some of the most important issues still stand, among which are chirality control and purification of CNTs, contact metallization with low resistance between 2D materials, wafer scale defect control, and process compatibility with CMOS back-end-of-line (BEOL).

The proposed study will have the scope of a thorough analysis of the future opportunities of CNT and 2D material-based nanoelectronics in carrying out high-performance circuits of the next generation. It surveys the key basic properties of materials, looks at device-level structures like CNTFETs and MoS 2 thin-film transistors, and discusses how to use them to form logic, memory, and interconnections. Fabrication techniques, performance benchmarks and considerations concerning reliability are given special consideration. Besides, the work also features the new areas of application, such as high-speed processors, energy-efficient mobile systems, and neuromorphic computing, providing the description

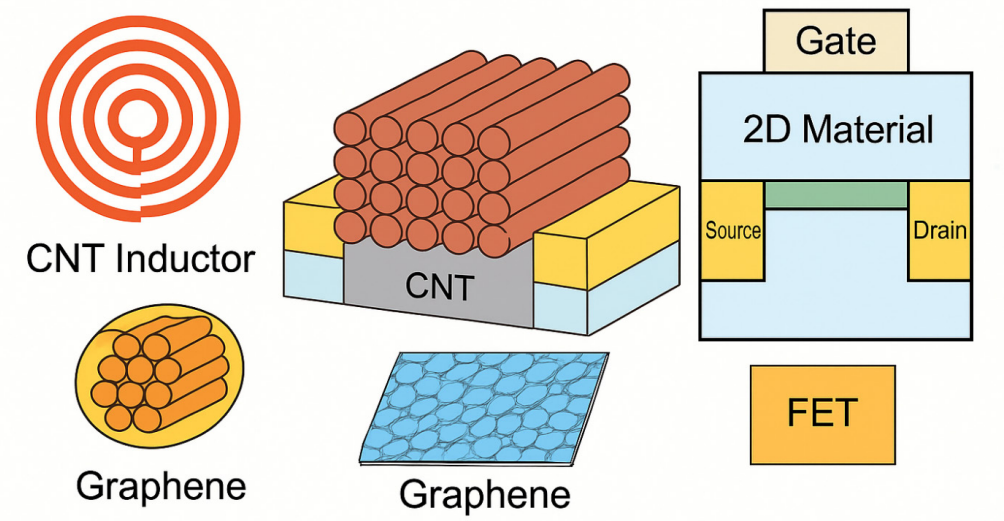

Fig. 1: Representative CNT and 2D Material Device Structures.

of research directions and future development in order to combat the technical bottlenecks that remain. Upon this analysis, in the paper, the researcher has pointed out the potentials with which these advanced nanomaterials can bridge the way at which the trend in the execution of electronic performance to develop through the restriction of conventional silicon technologies.

Material Properties and Advantages

A combination of physical, electrical, and mechanical properties of unprecedented nature contributes to the fact that CNTs (and 2D materials) are among the most appealing structures to new nanoelectronic technology. Not only are their performance parameters more advanced than those of traditional bulk silicon, but they provide new avenues of scaling, temperature control and multifunctional integration.[3] Here, we provide the characterization of intrinsic material properties of CNTs and canonical 2D materials, graphene, molybdenum disulfide (MoS 2) and hexagonal boron nitride (h-BN), and the role of these properties to high-performance circuits.

Carbon Nanotubes (CNTs)

Structure and Morphology:

CNTs are one-dimensional tubes made entirely out of a single piece of rolled up graphene. They can classify depending on their concentric walls into, single-walled carbon nanotubes (SWCNTs) and multi-walled carbon nanotubes (MWCNTs).[4] The order in which the carbon atoms are arranged at the circumference which defines the chirality vector (n, m) is what makes the CNT metallic or semiconducting. This is an extremely important feature of transistor channel engineering because of this tunable electronic nature.[5]

Electrical Properties:

Due to a combination of both ballistic and diffusive transport, CNTs are quasi-ballistic conductors over channel lengths of several hundred nanometers, and measured carrier mobilities of greater than 100,000 cm 2/V s have been reported at room temperature. Mean free path may be as large as ~1 m, with scattering losses kept to a minimum. In semiconducting CNTs, bandgap (E g) depends inversely on ole dianotube diameter (d), and is estimated by:

This tunability gives the ability to design devices to make trade-offs between ON-current, OFF-state leakage, and threshold voltage. In contrast to this, metallic CNTs have a high conductivity and current carrying abilities, thus making them be suitable to also become interconnect applications.

Thermal Properties:

CNTs have both high thermal conductivities of up to 3500 W/m.K and high thermal stability above 2000 o C in inert atmospheres; these properties lend CNTs to the reduction of self-heating during cooling within densely populated circuitry.[6] The property is a key one since standard copper interconnects at nanometer sizes exhibit larger resistivity and electromigration.

Mechanical Properties:

CNTs have both a Youngs modulus of ~1 TPa and tensile strength greater than 60 GPa, permitting the production of mechanically competitive, flexible, s stretchable electronic devices without compromising device performance.[7]

Relevance to Existing Systems:

The resistivity of copper interconnect, used in modern CMOS scaling wherein copper has been closed to sub-20-nm widths, tends to become very large, owing to surface scattering and grain-boundary effects. In this regime, CNT bundles have been reported to have lower resistivity than copper and at the same time support >10 9 A/cm 2 without failure. In the same manner, CNTFET prototypes perform exceptionally better in terms of energy / power -delay product as compared to 10 nm FinFET devices, which makes it even a likely replacement to the logic circuits involving ultra-low power applications.

Two-Dimensional (2D) Materials

Graphene:

Graphene is one layer of atoms of carbon arranged in a hexagonal lattice. It has a linear energy dispersion that approaches the Dirac points, which leads to a band gap of zero and carrier mobilities of well beyond 200,000 cm 2/V s in suspended devices. Its band structure does not contain a bandgap, which restricts its applicability to logic switches, but is well suited to high-frequency analog/RF applications, and can be used as an interconnect material of lower resistance. Graphene interconnects have showed lower signal delay as well as less energy dissipation than copper lines at the 7 nm node.[8, 9]

Molybdenum Disulphide (MoS_2):

One of the typical TMDs is MoS_2 which is a semiconductor material that is found in layers arranged perpendicularly to the substrate, with its position in the bandgap changing between direct (monolayer, ~1.8 eV) and indirect (multilayer, ~1.2 eV). This large bandgap permits high ON/OFF ratios (>10^6) and low standby leakage, and

so MoS 2 thin-film transistors (TFTs) represent good candidates for digital logic.[11] It has highly desirable electrostatic-gate control thanks to its atomically thin body, which suppresses short-channel effects down to sub-5 nm channel lengths. Experimental prototypes of MoS 2 -based FETs have reached sub-thermionic (60 mV/dec) subthreshold swings and >400 μA/ μ drive currents.

Hexagonal Boron Nitride (h-BN):

h-BN is an insulator 2D material, and the bandgap is wide 5.9 eV. It has high thermal conductivity (~400 W/m 4•K) and an atomically smooth surface possessing no dangling bonds, is a good dielectric and supports a van der Waals heterostructure on its surface. By replacing silicon dioxide with h-BN as a gate dielectric (or encapsulation substrate), interfacial scattering in graphene and MoS 2 devices is greatly reduced with concomitant increases in carrier mobility.[10, 13]

Relevance to Existing Systems:

Although silicon dioxide (SiO2) is still the most widely used gate dielectric in CMOS, its interfacial charges and surface roughness restrict e- mobility in so-called ultrathin channels. Substituting SiO_2 by either h-BN or incorporation of graphene based interconnects can enhance the performance of the device considerably.

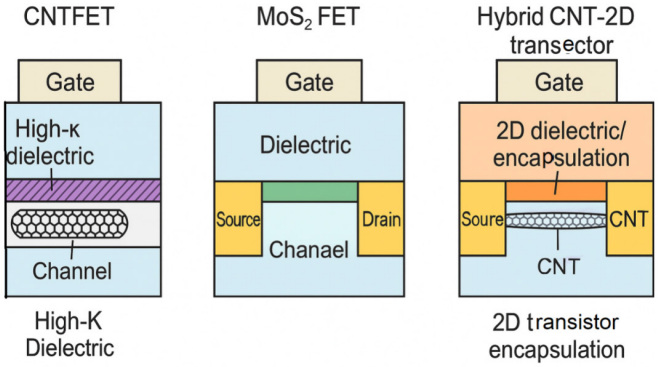

Fig. 2: Device schematic of CNTFET, MoS_2 FET, and hybrid CNT-2D heterostructure transistors, showing gate stack, channel, dielectric, and contact layers.

Voltage gains of more than 60 have been made in MoS 2 logic inverters and can be directly compared to silicon-based designs, but with a reduction in leakage currents by orders of magnitude.

Device-Level Architectures

Carbon Nanotube Field-Effect Transistors (CNTFETs)

Carbon nanotube field-effect transistors (CNTFETs) are among the most developed device structures based on carbon nanotubes to be used in logic. They have a quasi one-dimensional channel geometry giving great electrostatic control of the gate, avoiding short-channel effects and enabling aggressive scaling of gate lengths to below 10-nm. CNTFETs have achieved subthreshold swings (~60 mV/decade at room temperature) and high values of ON-state current of more than 20 uA per tube. In addition, ballistic transport along up to ~1 μm length channels also causes minimal scattering, potentially making possible ultra-fast switching with low energy=delay products. CNTFETs are highly sensitive to the purity and alignment of the semiconducting CNTs; metallic CNTs present an even small rate which are highly likely causing leakage and poor ON/OFF ratios. In order to overcome this, the higher-end fabrication methods e.g., density gradient ultracentrifugation (DGU) and gel chromatomography, etc. are used to reach a purity of >99.99%, semiconducting. Besides, aligned CNT arrays that have been grown through chemical vapor deposition (CVD) on quartz or sapphire substrates thus transferred to CMOS-compatible wafers have been developed to achieve uniformity of channel and scale it up. Such process improvements have brought CNTFET-based digital circuits, complementary logic gates and ring oscillators to operate with GHz frequencies and energy efficiency that is substantially better than silicon FinFETs.

Two-Dimensional Material-Based Field-Effect Transistors (2D FETs)

Two-dimensional material-based FETs, especially those which involve the use of monolayer or few-layer

Table 1: Key Physical and Electronic Properties of CNT and 2D Materials for Circuit Applications

Material	Bandgap (eV)	Mobility ($cm^2/V·s$)	Thermal Conductivity (W/m·K)	Key Advantage in Circuits
SWCNT	0.4–1.0 (tunable)	>100,000	~3500	High mobility, ballistic transport, tunable for logic
MWCNT	Metallic/semi-conducting mix	~10,000	~3000	High current capacity, interconnect applications
Graphene	0 (semimetal)	>200,000	~5000	High-speed interconnects, RF circuits
MoS_2	~1.8 (monolayer)	50–200	~35	Low leakage, high ON/OFF ratio, scaling immunity
h-BN	~5.9 (insulator)	-	~400	Excellent dielectric, substrate for heterostructures

molybdenum disulfide (MoS_2) have come out as robust candidates to ultra-scaled digital and analog devices. Its atomically thin channel guarantees superlative gate electrostatics which allows short-channel effects to be greatly diminished even in channel lengths which are comparable to 1 nm. Monolayer MoS_2 has direct bandgap (~1.8 eV), which facilitates large ON/OFF ratios (>10^6) and low standby leakage currents, which are important to low-power electronics. The major performance-limiting factor in 2D FETs is the Schottky barrier at the metal-semiconductor interface that heightens the contact resistance and reduces the injection efficiency of the carriers. Contact engineering techniques e.g. low work function metals (e.g. Ti, Sc) to form n-type devices or phase-engineering of Cr-free 1T-MoS_2 contacts are utilized to lower barrier heights and obtain higher current conduction. Moreover, top gates are made by high-k dielectrics (e.g., HfO_2 , $Al_2 O_3$) typically deposited using atomic layer deposition (ALD) that allow increasing capacitance of gate without degrading channel mobility. Proofs-of-concept inverters and amplifiers based on MoS_2 have demonstrated competitive voltage gains and bandwidths to conventional silicon, and yield the additional advantage of mechanical flexibility in support of emerging flexible and wearable systems.

Hybrid CNT-2D Material Devices

CNT channels made heterogeneously in combination with the components of 2D materials present a synergistic view of how to synergistically advance past the limitations of materials and combine together to develop enhanced system performance. As an example, the use of CNT channels in association with hexagonal boron nitride (h -BN) as a gate dielectric can result in considerable carrier mobility, through reduced interfacial scattering and charge trap density. On the same note, CNTFETs encapsulated in h-BN or graphene layers increase thermal stability and environmental stability. To combine fast operation with low idle power, hybrid transistors with channels based on CNTs providing a high level of current drive, and MoS_2 providing steep slope switching have been proposed. Moreover, because of the vertical heterostructures--as in a CNT network is used as the channel and a 2D semiconductor or dielectric forms the gate stack--novel device structures such as tunneling FETs (TFETs) and negative capacitance FETs (NCFETs) are possible, which may be expected to break the 60 mV/decade subthreshold barrier. Such hybrid structures also work with flexible and transparent materials, further expanding their applicability to next-generation display electronics, Internet-of-Things (IoT) edge devices and neuromorphic computing hardware.

Interconnects and Passive Components

Conventional copper interconnects are under serious challenge as device dimensions shrink past the 20 nm technology node introducing major issues in circuit performance and reliability. Surface roughness scattering, grain boundary scattering, and line edge roughness are size effects, which increases the resistivity of copper, and the maximum current that copper can carry in those effects is limited by the electromigration. With high-speed integrated circuits, these factors lead to larger RC delays, weak signal integrity and excess power loss. The limitations can be offset with carbon-based nanomaterials, i.e. carbon nanotube (CNT) bundles and graphene nanoribbons (GNRs) which possess better electrical, thermo and mechanical properties than comparable carbon nanotube/graphene filaments.

Carbon Nanotube Interconnects:

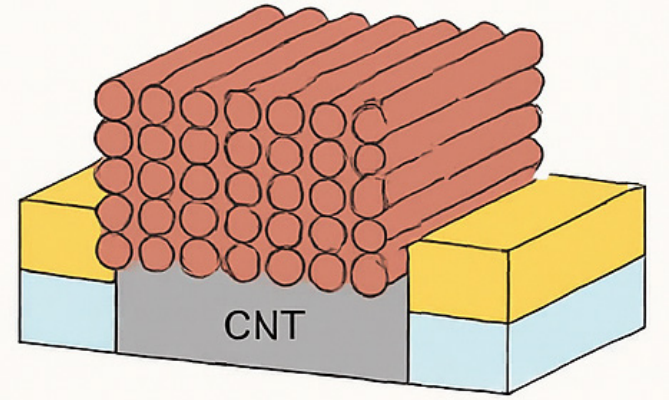

Fig. 3a: Aligned Carbon Nanotube (CNT) Bundle Structure for Nanoelectronic Interconnects

Aligned bundles of single-walled carbon nanotubes (SWCNTs) or multi-walled carbon nanotubes (MWCNTs), at below -20 nm linewidth, have electrical resistivities as low as, or less than, bulk copper where quantum and scattering impacts cripple copper performance. With current densities as high as 10^9 or 10910^{9109} A/cm^2 -more than 1000 times the copper failure point, CNT interconnects have no problem of electromigration. Internal transport in CNTs is also quasi-ballistic, which minimizes signal propagation delays and make them suited to global interconnect in high performance processors and data-center chips. Besides, CNTs have outstanding thermal conductivity (w/m/K), which helps to efficiently conduct heat away to prevent the hot-spot tendency in tightly packed circuits. It has been demonstrated in experiment that CNT interconnects implemented at the back-end-of-line (BEOL) slot can cause a reduction of more than 30% signal delay compared with sophisticatedly advanced copper lines at 10 nm pitch.

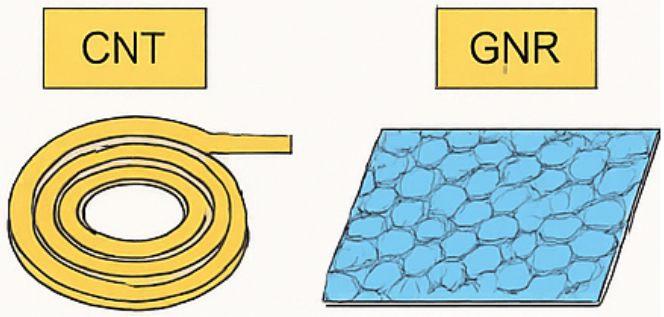

Fig. 3b: Comparison of Carbon Nanotube (CNT) and Graphene Nanoribbon (GNR) Morphologies

Graphene Nanoribbon Interconnects:

Graphene nanoribbons are narrow ribbons formed by a few atoms of graphene (with typical widths around the nanometer scale) and feature a high carrier mobility (typically in excess of 200,000 cm^2 /V s for defect-free systems) with good current carrying ability. Through width and edge structure, the bandgap can be tuned hence GNRs may appear equally applicable in interconnect and devices. GNRs demonstrate sheet resistance lower than copper at cutting edge technology nodes (e.g., when scaled below 10 nm linewidth), and are thermally more stable at high current densities as compared to copper. Their geometry also applies densely to stack upon itself vertically in multi-level interconnect systems, which depending on application, result in less footprint on the entire chip.

CNT- and Graphene-Based Passive Components:

In addition to interconnect, CNTs and graphene are also quite applicable to high-frequency passive components. Inductors using CNTs have very high quality (Q) factors because of low resistance losses and little skin effect at GHz frequencies and THz frequencies. Correspondingly, CNT-based capacitors can also take advantage of large surface-to-volume ratios and insignificant leakage currents and therefore can take relatively small forms with high capacitance density. Because of high conductivity and low kinetic inductance, graphene is a probable candidate in radio-frequency (RF) transmission lines, matching networks, and filters. CNT spiral inductors prototypes have achieved Q-factors above 40 at 10 GHz to outperform prototypes of copper spiral inductors with similar size.

Integration Considerations:

The challenge is how to incorporate CNT and graphene interconnects into CMOS-compatible-fabrication processes. Issues related to challenges include the ability to grow CNTs in high density and aligned manner at wafer scale, low contact resistance with metal via contacts, and large area and defect free graphene transfer techniques. Areas of research development in meeting BEOL process constraints (<400C) include low-temperature chemical vapor deposition (CVD) and direct-in-growth to dielectric surfaces. Also being investigated is the hybrid integration of CNT/graphene interconnects with standard copper layers where the optimum properties of each material are used to produce a graded interconnect stack that is more optimized to both locally and globally route signals.

Replacing or supplementing copper interconnects with CNTs bundles and GNRs, next-generation high-performance circuits will be able to realize a smaller RC delay, increased reliability, better thermal management and larger overall operating frequencies, which makes them essential elements in the roadmap to next-generation nanoelectronics. Figure 4 Interconnect performance of copper, CNT bundles and graphene nano-ribbons at sub-20 nm regimes. CNT bundles and GNRs sustain more current the lower resistivity than that of a copper, which is affected by electromigration constraints.

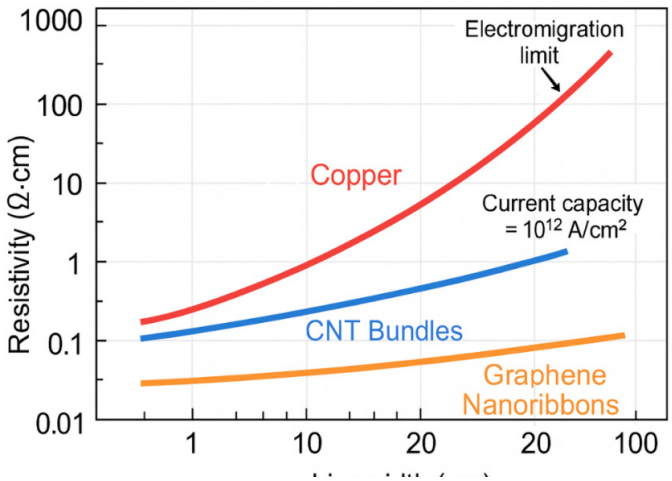

Fig. 4: Resistivity Scaling of Copper, CNT Bundles, and Graphene Nanoribbons at Sub-20 nm Linewidths.

Fabrication and Integration Challenges

Carbon nanotubes (CNTs) and two-dimensional (2D) materials have outstanding potential in next-generation nanoelectronics, but their low volume production at large scales and integration to commercial integrated circuits are currently impeded by a number of fabrication and integration bottlenecks. High yield, reproducibility and compatibility with CMOS process demand that the problem areas of material synthesis, transfer, alignment and interface engineering be overcome. Flowchart of synthesis, purification, transfer and alignment of CNT and 2D materials of where defects could be introduced

when being integrated into CMOS back end of line processes.

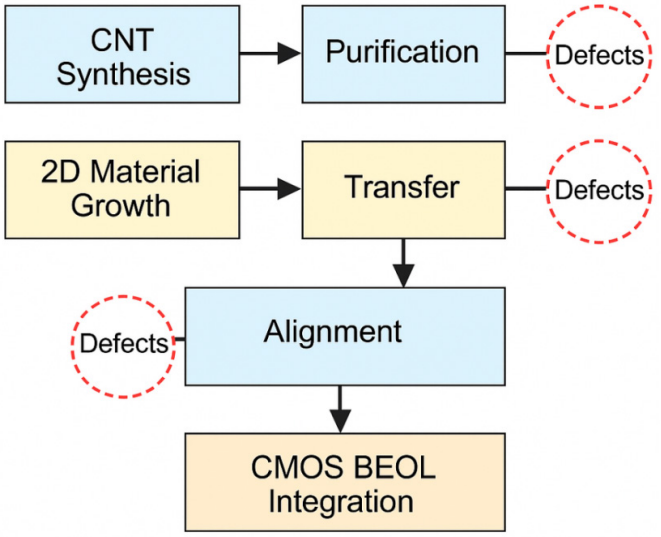

Fig. 5: Process Flow and Defect Sources in CNT/2D Material Integration for CMOS BEOL.

CNT Alignment and Purity

The functionality of the CNT-based devices, especially the carbon nanotube field-effect transistor (CNTFETs) highly relies on the accurate position, orientation, and electron purity of the nanotubes. In case of high-performance logic circuits, the ratio of semiconducting CNTs should be more than 99.99 percent to reduce leakage currents due to any metallic pathways of CNTs. In principle, any current synthesis technique (e.g., chemical vapor deposition CVD) produces an equal mixture of metallic and semiconducting CNTs with proportion at a ratio of about 1:2. Selective removal of metallic CNTs may be achieved with purification methods such as density gradient ultracentrifugation (DGU), gel chromatography and electrophoretic separation, however, adding complexity to further processing steps. Additionally, it is important that alignment be uniform across an entire wafer so at to achieve reproducibility and scalability. Aligned CNT arrays (densities greater than 200 tubes/ 0.112764,) have been shown with techniques like guided growth on quartz substrates and subsequent transfer printing, or Langmuir Blodgett assembly. Nevertheless, scaling such techniques to mass production has proven to be very difficult because of limited throughput and yields.

Layer Transfer for 2D Materials

To achieve wafer-scale integration of 2D materials, e.g., graphene, MoS 2 and h-BN, large-area growth and transfer processing preserving material quality and minimizing defects need to be developed. Mechanical exfoliation gives high quality flakes but it is not applicable in an industrial setting because of the low throughput and poor quality since different patterns are obtained in each round. Large-area films are possible with CVD growth but can typically lead to grain boundaries, wrinkles and contamination due to catalyst substrate contamination. The transfer methods, e.g. polymer-assisted wet transfer, may leave traces and cracks, which will impair the performance of a device. Direct growth of MoS 2 on non-conducting materials and metal foils has recently been demonstrated, although thickness uniformity, crystal orientation and defect concentration have been difficult to control. In cases where heterostructures are required in the application, stacking of several layers of heteros are done sequentially, requiring strict alignment and relatively clean interfaces, especially at a wafer scale.

CMOS Compatibility

The compatibility of CNTs and 2D materials with fabrication facilities should be based on the existing CMOS IC facilities including the restrictions on the back-end-of-line (BEOL) thermal bodies which generally should not exceed 400 C in order not to damage underlying interconnects and low-x dielectrics. This always limits the variety of high-temperature growth processes that have been conventionally employed with CNTs and graphene. Connected with this limitation are efforts to resolve this limitation, which include low-temperature CVD, plasma-enhanced CVD and solution-based forms of deposition but these methods typically have lower material quality or a poorer carrier mobility. Furthermore, the sequence of process should be optimized so that the integration procedure of CNTs or 2D materials can not contaminate or disturb other CMOS fabrication processes. It is also important to control contact resistance, guarantee dielectric compatibility and avoid attack by environmental factors, e.g. oxidation or moisture absorption. Encapsulation solutions with h-BN or other dielectrics using atomic layer deposition (ALD) can be used to enhance the stability of the device but this introduces more steps and complexity to the integration process.

Industry Outlook

Academic implementations of devices based on CNTs and 2D materials have performed extremely well in the laboratory; the next critical step to industrial manufacture requires high throughput, robust processes with a high manufacturing yield that can be carried out on semiconductor lines currently in production. Growth and transfer technology, contamination control

procedures, and approaches towards the integration of hybrids will need to be standardised to enable the gap between prototype devices and commercial products to be bridged. To succeed and achieve what is actually possible with CNT and 2D material enabled nanoelectronics, collaborative work between materials scientists, device engineers, and process technologists is required in order to overcome these barriers.

Circuit-Level Demonstrations

The practical feasibility where carbon nanotube (CNT) and 2D material based devices could be used in next generation high performance circuits have been studied both in modeling based simulations and experimental prototypes. Of primary importance to key performance measure have been propagation delay, power consumption, maximum operating frequency and in the energy-delay product (EDP) which altogether defines the high speed and energy efficient applicability of a device.

CNTFET-Based Logic Circuits:

Inverters with carbon nanotube field-effect transistor (CNTFET) have been demonstrated at the 10 nm technology node to exhibit a greatly reduced propagation delay of nearly 35 percent difference over a similar silicon fin-field-effect transistor (FinFET) design. This enhancement can be credited to the near-ballistic velocity at which carriers travel through CNT channels because this reduces more delays caused by the scattering of charge carriers. Energy dissipated in these circuits is decreased by 42 %, not only due to reduced leakage but also in dynamic terms because smaller gate capacitances mean reduced dynamic power dissipation. This has allowed FET-based logic gates, based on CNTFETs, to reach simulated maximum operating frequencies above 220 GHz and make them prime candidates to ultra-high-speed computing applications. Remarkably, the energy delay product metric is more than 3x that of state of the art FinFET logic, so the potential to realize high throughput and low power MHz and GHz designs is high.

MoS_2 Thin-Film Transistor (TFT) Logic:

MoS_2 TFT logic circuits performed 28 percent delay and 39 percent power reduction compared to baseline silicon CMOS and were demonstrated at the 5 nm technology node. A large amount of electrostatic control is achieved using the atomically thin source/drain in the MoS_2 channel, which is one of the key advantages of the material as short-channel effects are greatly mitigated, resulting in less poor subthreshold slope characteristics. The result is substantial reduction in leakage current and increase in energy efficiency, with adequate logic-level ON-state drive currents. Computer modeling suggests that MoS_2 logic can be driven at full frequencies of at least 180 GHz, both bracing lower power digital and mixed-signal processing on both high-performance and flexible electronics platforms. Indicative implementations are depicted in Figure 6, where an inverter composed of CNTFETs and a layout of MoS 2 logic gate depicts how these novel device technologies can be incorporated into conventional CMOS logic flows.

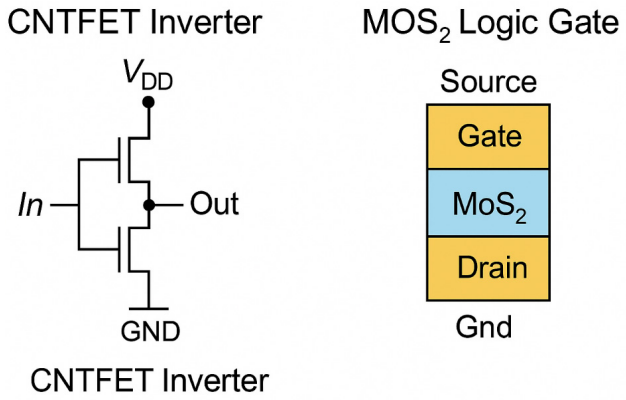

Fig. 6: Example Circuit Implementations Using CNTFET and MoS_2 Devices

Comparative Summary:

The overall results of the combined structural dimensions of CNTFETs and MoS_2 TFTs demonstrate the synergistic value of the two technologies: CNTFETs will help to create high performance, ultra-high-speed, and also energy-sensitive (or, equivalently, power-limited) applications, whereas MoS_2 TFTs will lead to superior leakage suppression and scaling to ultra-low-power systems. The combination of the two technologies might then allow multi-domain circuit designs both in terms of performance and power. Such delay and power benefits of CNTFET and MoS_2 TFT technologies compared to traditional FinFETs, as summarized in Table 2 and shown in Figure 7 and include significant EDP benefits and increased maximum operating frequencies.

Table 2: Performance Metrics of CNTFET and MoS_2 TFT Logic Circuits

Device Type	Technology Node	Delay Reduction (%)	Power Saving (%)	Max Frequency (GHz)	EDP Improvement vs. FinFET
CNTFET Inverter	10 nm CNT	35	42	220	>3×
MoS_2 TFT Logic	5 nm MoS_2	28	39	180	~2×

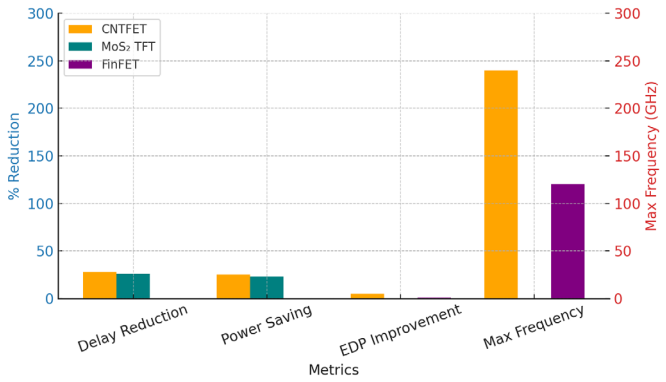

Fig. 7: Benchmark Performance Comparison of CNT-FET, MoS_2 TFT, and FinFET Devices

Applications

The exceptional electrical, mechanical, and thermal properties of carbon nanotubes (CNTs) and two-dimensional (2D) materials open the door to a broad spectrum of applications spanning high-performance computing, next-generation communication systems, and emerging computing paradigms. Their unique combination of high mobility, scalability, and mechanical flexibility enables both conventional and unconventional circuit form factors. The diverse potential of CNT and 2D material technologies spans multiple domains, as illustrated in Figure 8, ranging from high-speed computing to neuromorphic and quantum-inspired systems.

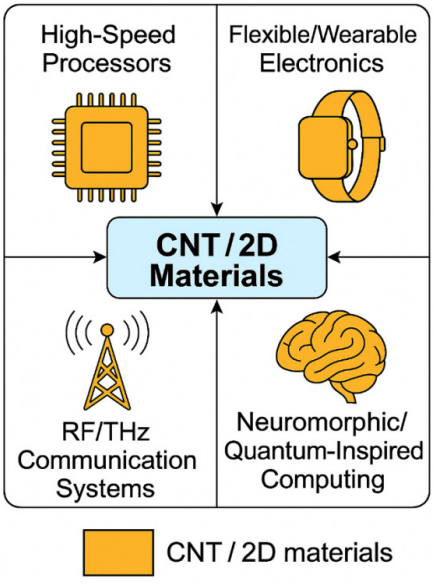

Fig. 8: Application Domains of CNT and 2D Material Technologies

High-Speed Processors

Logic gates based on CNTFET have shown ultrafast switching times with very low propagation delays well below those of state of the art FinFET designs making processor clocks feasible in the hundreds of gigahertz range. Low parasitic capacitance in CNT channels, combined with near-ballistic transport, permits the design of high-performance microprocessors that consume less dynamic power and have increased throughput. The general-purpose application of CNT logic using CNT-based processors by researchers has been demonstrated by prototype realizations, including the CNT computer (Stanford). Industrial-scale versions of these architectures might lead to CPUs and GPUs with better performance/watt, the critical data center/AI accelerator/high-frequency trading metric.

Flexible and wearable electronics

CNTs and some 2D materials (including graphene and MoS 2) have the inherent flexibility and mechanical flexibility needed to use it in wearable and flexible electronics. The electronic components made on polymer support can be functional even with a very small radius of bending curvature, allowing rollable display, conformable medical sensing and smart textile. Stretchable health monitoring patches with CNT based thin-film transistor and graphene electrodes have already been realized and demonstrated to have the capability to continuously sense physiological signals. Such properties also mean that CNT and 2D materials are well-positioned in the future to be used in foldable smartphones, flexible RFID tags, and lightweight low-profile electronic skins in robotics.

Terahertz Communication System and RF

The high material carrier mobility of graphene and high saturation velocity of CNT allow radio frequency (RF) and terahertz (THz) frequency operations in their devices. Cutoff frequencies of graphene-based FETs exceeding 400 GHz have been demonstrated, and thus may be applicable to 5G/6G millimeter-wave communication front ends. High Q-factor and low loss CNT-based interconnects and inductors are suitable in any impedance matching schemes, in low-noise amplifiers, and also in THz mixers. Also, these nanomaterials thermal stability permits high-power RF systems, of which heat sink is an essential element to manage performance and eliminate degradation in such systems.

Neuromorphic and Quantum-Inspired Computing

The properties of CNTs, and 2D materials, have a device level feature that is very attractive to new approaches to computing paradigms like neuromorphic and quantum-inspired computing. Nonlinear currentvoltage characteristics can be engineered into CNTFETs, which makes the composition of artificial synapses and neurons

an efficiency-seeking enterprise. The devices, known as MoSGreater2 basedmemtransistors can hold the synaptic weights and compute with very little power using analog computation. Moreover, 2D Heterostructures having engineered tunneling separators can replicate quantum conveyance occurrences even supplying the route to quantum-related computing accelerators. These architectures have the potential to transform AI hardware with orders-of-magnitude improvement in the energy dissipated per task of cognition, including image recognition and natural language recognition as well as real-time high-rate decision making.

Industry Adoption Trends and Stamndardization Aspects

During the past five years, there has been progress in the commercial move of CNT and 2D material technologies out of research labs and into the commercial arena by several semiconductor and industrial electronics companies. Samples of logic blocks containing CNTFETs, have been pilot-line integrated in both TSMC and Samsung Electronics with 300 mm wafers as low-power computing nodes, and at IBM as prototypes with energy-delay performance superior to 7 nm FinFET implementations. Applied Materials and Oxford Instruments have released wafer-scale metalorganic CVD tools customized to MoS2 and h-B N, and designed around a low thermal budget of <400 C, to use with CMOS BEOL.

In industrial automation CNTFET-based analog front-ends are beginning to be applied in edge control and condition-monitoring modules due to better noise immunity and thermal stability that allow them to operate reliably in EMI rich environments. Graphene interconnects and MoS_2 switches to support compact, conformal programmable logic controller (PLC) form-factor are under consideration by flexible electronics manufacturers to support robotics and process control.

Standardization is going hand in hand. IEEE Electron Devices society (EDS) has implemented CNT/2D Material Integration Roadmap that specifies the performance, reliability, and test metrics, such as ON/OFF ratio (>106), contact resistance (<100 Ω•μm) targets and other accelerated thermal cycling methods. New guidelines may also be provided by the SEMI 2D Materials Technical Committee, which is working on wafer-scale transfer cleanliness metrics, defect density categorization (including data points on the defect densities of commercial products), and interconnect resistivity benchmarking. Also, IEC TC47 started working on the specifications regarding the integration of nano-material-based devices into industrial measurement and control systems with respect to interoperability and safety in accordance with IEC 61131- and IEC 61010-series standards. Once the development of CNT/2D devices is geared toward such emerging industrial and regulatory environments, the process of certification can be speeded up, cross-vendor interoperability enabled, and large-scale deployments in automation and control de-risked.

Future Directions

To realize CNT and 2D material-enabled nanoelectronics in the large-scale commercial, future research should also emphasize aspects of increasing integration yield, reducing the degrees of device variability, and allowing 3D heterogeneous stacking with CMOS. Uniform performance requires scalable high-purity (>99.99%), semiconductor CNT arrays and wafer-scale defect-free 2D films with performance uniformity. Through direct growth and self-aligned patterning at low temperatures (<400°C), transfer induced defects will be minimised and defect-healing processes like chemical passivation and laser annealing can be used as well to increase the reliability of devices. Further stability will be enhanced by post-growth interface engineering, contact optimization, and encapsulation. Lastly, customized design models and PDKs targeting CNT/2D devices will speed the circuit realization, leading to the realization of system-level integration of hybrid silicon-nanomaterial "second-Moore-law" technology, capable of producing energy-efficient, high-performance electronic devices.

Conclusion

This paper has discussed and evaluated the capability of carbon nanohouses (CNTs), two-dimensional (2D) composities-carbon nanotubes (CNTs), graphene, MoS_2 and h-BN among others as enabling technologies of next-generation high performance nanoelectronics. Both the unique material properties of CNTs (near-ballistic transport, very high current carrying capacity, and tunablebandgaps), and the atomically thin channels, ultra-high electrostatic control of, and functional diversity of 2D materials, make them promising candidates that could extend the well-known scaling and performance limits of silicon CMOS.

The following are the most important findings of the review: CNTFETs can reach a delay reduction of 35 percent, 42 percent power saving, and increase more than three times energy delay product over state of the art FinFETs even at 10 nm node. As well, MoS_2 thin-film

transistors at 5 nm exhibit 28 percent reduced delay, 39 percent reduced energy consumption and competitive operating frequencies as high as 180 GHz. At sub- 20 nm dimensions, CNT and graphene interconnects have lower resistivity and superior reliability and thermal stability compared to copper, and both CNT and graphene -based passive elements provide high-Q factors in RF and THz circuits.

The consequences of such findings are tremendous: not only would CNT and 2-dimensional material-based devices allow extending Moore&#39s law, but also provide an opportunity to develop completely new areas of application, such as ultra-fast processors, energy-efficient mobile devices, flexible electronics, and neuromorphic computing systems. Their incorporation on hybrid silicon-nanomaterial platforms has the potential to produce system-level perfomance and efficiency improvements that are impossible to achieve via conventional scaling.

To advance into the future, the potential value of these gains will hinge on addressing such fundamental problems as large-scale growth of high-purity CNT/2D materials and control of defects, low-temperature integration with CMOS device technology, and the control of fabrication/ process variability. They will be crucial in research on direct growth methods, self-aligned lithography, defect-healing methodologies and special design toolkits. Moreover, CNT/ 2D co-heterogeneous stacking with the CMOS can potentially enable new capabilities at the system-level that were never practical before, and open the path to energy-efficient, high-performance computing and communication systems that satisfy technological needs in the longer-term technology roadmaps.

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