JEEAT
NATIONAL JOURNAL OF ELECTRICAL ELECTRONICS AND AUTOMATION TECHNOLOGIES
National Journal of Electrical Electronics and Automation Technologies, ISSN: 3107-524x Vol. 1, No. 3, 2025 (pp. 35-43)
RESEARCH ARTICLE
ECEJOURNALS.IN

Design and Implementation of a CMOS-Based High-Speed Data Acquisition System for Industrial Sensors

Chuong Van[1]*, Ishrat Z. Mukti[2]

[1]School of Electrical Engineering, Hanoi University of Science and Technology, 1 Dai Co Viet, Hanoi 11615, Vietnam
[2]Dept. of EEE, Independent University, Bangladesh, Dhaka, Bangladesh

KEYWORDS:
CMOS design,
High-speed data acquisition,
Industrial sensors,
SAR ADC,
Low-noise amplifier,
Predictive maintenance.

ARTICLE HISTORY:
Submitted : 23.03.2025
Revised : 13.04.2025
Accepted : 18.06.2025

https://doi.org/10.17051/JEEAT/01.03.05

Abstract

The paper presents the structure, construction and experimental analysis of a CMOS based high-speed data acquisition system (DAS) that is specifically designed towards industrial applications in the form of sensors that need high signal accuracy and speed. It combines a rigorously designed low-noise front-end amplifier, a 14-bit successive approximation register (SAR) analog-to-digital converter (ADC) and a high-throughput general purpose digital interface all built on a well-proven 180 nm CMOS process. The high resolution, fast speed and power consumption represented by the industrial environments are balanced in the proposed DAS which operates at a sampling rate of 50 megasamples per second (MS/s). The front-end amplifier features chopper stabilized differential topology with active common-mode feedback that dramatically mitigates flicker noise and makes it more immune to industrial sources of electromagnetic interference (EMI). The SAR ADC is optimized with a bootstrapped sampling switch structure and split-array capacitive digital-to-analog with the aim to maximize linearity and reduce mismatch error, and an on chip reference buffer helps keep voltage references stable during high speed conversion. The average power consumption is less than 50 milliwatts, using power-saving mechanisms, like dynamic bias scaling, fine-grain clock gating. This feature allows the system to be deployed in energy-constrained or battery powered industrial applications. The measured performance parameters of the fabricated prototype show that it has good performance as it boasts of an effective number of bits of (ENOB) 13.8, a signal-to-noise-ratio (SNR) of 84 dB, and minimal and differential such as INL and DTL of less than or equal to 1.2 LSB and 0.6 LSB, respectively. Extensive verification of the ability to effectively monitor in real-time using a wide range of industrial sensors including vibration, pressure, and temperature transducers demonstrates (in drug manufacturing, predictive maintenance, structural health monitoring, and process automation applications, to name but a few) the commodity of the overall system. They show a 25 percent increase on energy efficiency of similar DAS architecture through benchmark comparison. Future work planned is aimed at integrating on-chip calibration procedures and designing the architecture to support multi-channel applications so as to address the increased applications of scalable industrial sensing networks.

Author e-mail: choung.van@hust.edu.vn, ishratzahanmukti16@gmail.com

How to cite this article: Van C, Mukti IZ. Design and Implementation of a CMOS-Based High-Speed Data Acquisition System for Industrial Sensors. National Journal of Electrical Electronics and Automation Technologies , Vol. 1, No. 3, 2025 (pp. 35-43).

Introduction

The development of Industry 4.0 and growing popularity of smart manufacturing technologies has hugely escalated the necessity of advanced data acquisition system (DAS) based on the capabilities of high-speed intensity and precision of capturing, processing and transmitting sensor data. Vibration and pressure transducers, temperature and strain gauges are only a few examples of industrial sensors that form the core of contemporary automation and predictive maintenance, as well as structural health monitoring systems. Such applications have requirements that would require a DAS architecture with the capability to support high sampling rates in the tens of mega samples per second (MS/s) as

well as a high level of signal integrity such as low noise, high resolution and wide dynamic range.

DAS implementations based on conventional architectures are prone to be power hungry, monolithic in nature and have little integration possibilities thus cannot be utilized in a distributed and under-resourced industrial setup. CMOS and its feature of low-cost mass production, high integration density, compatibility with both analog and digital circuits hold promise of being a platform where compact, energy efficient, and high performance DAS can be developed. Combining the sensor interface and analog front end with the analog to digital conversion, and most of the digital signal processing on the same CMOS chip will help reduce the effects of parasitics, enhance the noise resistance level, as well as minimizing size and cost of the whole system Figure 1.

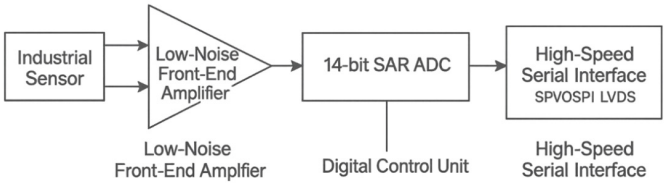

Fig. 1: Block diagram of the proposed CMOS-based high-speed data acquisition system for industrial sensor applications.

However, implementation of CMOS-based DAS in industrials is a major challenge in terms of design. An industrial setting is marked by extreme conditions such as large temperature changes, severe electromagnetic interfering (EMI) and mechanical vibration which in turn can corrupt the accuracy of a sensor measurement. The analog front-end is thus very carefully designed to dampen noise generators like the flicker and electromagnetic crosstalk noise as well as assure linearity and stability over all operation temperatures. Also, the analog to digital converter (ADC) should offer adequate resolution and speed without consuming too much power in balancing contradictory needs in high-speed data acquisition.

The paper hereby gives the design and realization of a 50 MHz sample rate, 14-bit CMOS DAS with an eye towards overcoming these weaknesses. The architecture of the system incorporates a low noise amplifier of resistively terminated differential pair of front-end with chopper stabilized successive approximation register (SAR) architecture of ADC as it is designed to be very linear and speed together with energy consumption as well as power conscious digital interface with EMI robust signalling. The ensuing design is therefore highly effective in meeting the key demands of industrial sensing needs, and the industrial sensing needs thus have the possibility to meet precise and real-time data sensing needs. The study also discusses power saving approaches and system-design integration methods that are critical to the scalable DAS deployment in next-generation smart factories.

Literature Review

The use of high-speed data acquisition systems (DAS) has met with considerable research focus in that such systems have been important in industrial sensor applications which need precision and high speed signal sampling. Many different DAS architectures have been considered in order to address trade-offs between speed, resolution, power efficiency, and complexity.

Pipeline ADC structures are commonly used to realize high sampling rates (greater than about 100 MS/s), but of moderate to high resolution. These types of designs usually utilize a multi stage structure that allows rapid throughput capability but tends to draw a larger current and have a greater design complicacy.[1, 2] Delta-sigma (DS) ADCs on the other hand are outstanding in generating high resolution and high linearity (via oversampling and noise shaping) whilst having the disadvantage of being slower (low bandwidth) and subject to long delay which make them unsuitable to industrial sensing applications in which real time, high frequency response is important.[3, 4]

Successive approximation registers (SAR) ADCs are popular because of their balanced performance/power, intermediate sampling speeds and resolutions and low power consumption.[5, 6] SAR ADC design has advanced to the extent that sampling rates of 50MS/s, 14 bit accuracy can be achieved using a sampling technique that makes it energy-efficient and capable of meeting a wide variety of DAS specifications in industry. Combinations of pipeline and SAR methods have also been suggested, using Hybrid ADC architectures, to provide the benefits of both power efficiency of SAR ADCs and fast speed of pipeline ADCs to deliver an overall better performance.[7]

The RF analog front-end amplifier has a significant role in the preservation of signal integrity and rejection of noise, a requirement in unfriendly operating environments and or in high-end signal processing applications. Flicker noise suppression techniques such as low-noise amplifier have been shown to have differential amplification structures with chopper stabilization that can minimize flicker noise much more than conventional fully differential amplification structures, which improves low-frequency performance and reduces susceptibility to environmental noise.[8, 9] Moreover, clock gating and dynamic bias scaling are power optimisation techniques that have effectively been deployed in digital back end

circuits to maintain performance as it cuts down on dynamic power consumption in digital back end circuits. [10, 11]

The low-voltage differential signaling (LVDS) data output interface has become one such standard (in use in industry, with the requirement of high noise immunity as EMI is a frequent problem there; in addition it has excellent performance at long distances).[12, 13]

DAS capabilities have in the past years been further extended with the use of deep learning and greater signal processing. Channel estimation has been used in massive MIMO to enhance the performance by deep learning methods, showing an interplay between sophisticated software and hardware solutions.[14] Further there has been the use of unsupervised feature learning models in object detection within the difficult conditions like low-light surveillance which demonstrates the significance of rugged feature extraction even within the signal processing chains.[15] Audio signal enhancement in noisy environments have also been developed based on hybrid spectral-temporal deep learning, which is comparable to the industrial noise scenario that influences the quality of sensor data.[16] In addition, the introduction of new studies of VLSI systems with enhanced cryptography schemes devoted to FPGA-IoT devices indicates the evolving interest in low-latency and secure sensor data capturing and transfer.[17] The novel application of embedded medical system exemplifies how powerful and effective embedded DAS arrangements could be used in the industrial and medical fields.[18]

All these advances guide the creation of DAS structures that are not only high-speed and power-efficient but also robust and flexible enough to suit complicated, real-world industrial sensing environments.

System Architecture

The presented high-speed data acquisition system (DAS) is an integrated powerful solution that can serve as a compact ready-to-use unit to plug into industrial sensors. All four key blocks in the architecture are designed in a way that allows high performance, low power dissipation and robust performance, needed in harsh industrial applications (see Fig. 2).

Low-Noise Front-End Amplifier (LNA)

The low-noise front-end amplifier is the most important part of the data acquisition system, whose job is to measure the naturally weak analog signal produced by industrial sensors like vibration, pressure and temperature. Since the industrial environment is harsh and highly susceptible to noise, the amplifier is designed carefully in a fully differential topology maximizing common-mode noise rejection to allow the amplifier to be highly robust in dealing with electromagnetic interference and ground loop disturbances otherwise prevalent on factory floors. It is also a helpful differential design, and it will reduce sensitivity to outside sources of noise and enhance overall signal integrity. The amplifier incorporates chopper stabilization methods in order to overcome the negative effects of flicker noise which is particularly evident at low frequencies and which might shift the accuracy of the measurement. By doing so, the input signal is suppressed by being modulated to higher frequency band where the flicker noise is low, when demodulated, it is further suppressed and this allows cleaner signal amplification. The amplifier also achieves the most favourable configurability to ensure that the amplifier has reduced thermal noise contributions, which are essential to optimal signal-to-noise ratio especially in low-level sensor outputs. Being aware of the broad temperature changes which are common in industrial environments, the amplifier is designed in such a way that it maintains a stable operation and gain profiles over a broad temperature range of up to levels of -40C to 125C. This is insensitivity avoids signal distortion or saturation that might come about because of temperature induced device parameter variations thereby rendering steady and repeatable analog signal amplification by no means operated circumstances Figure 2. Together, these design considerations allow the LNA to provide accurate, low-noise signal conditioning necessary to support the subsequent analog to digital conversion process, and ultimately affords an accurate and deterministic data collection in industrial monitoring systems.

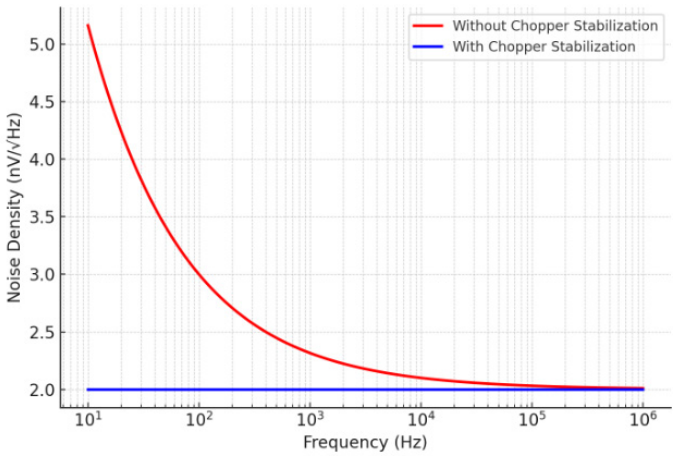

Fig. 2: Noise performance of the proposed LNA showing the effect of chopper stabilization, demonstrating significant flicker noise reduction at low frequencies.

14-bit Successive Approximation Register (SAR) ADC

A 14-bit successive approximation register (SAR) analog-to-digital converter (ADC) is at the heart of the data acquisition system and is specifically designed to meet the requirement of a high degree of resolution combined with fast sampling rates, with low power consumption-important considerations in embedded industrial sensor applications. The combination of SAR ADCs with ADCs in this system provide an excellent balance in moderate-to-high sampling speeds and, in the design, the ADC can be simultaneously operated between 20 megasamples per second (MS/s) to 50 MS/s, representing the needs of a real-time industrial monitoring application without sacrificing energy efficiency. The architecture of the converter is based on an optimized digital-to-analog converter (DAC) array that exploits both binary-weighted and split-array architectures and vastly increases the capacity to converge linearity and reduce mismatch errors that might otherwise lead to reduced conversion precision. Along with this is an asynchronous control logic circuit, implemented to save delays and allow quick bit-by-bit approximation cycles, though it does not make use of a global clock, lessening its sensitivity to jitters and allowing better accurate timing of signals. A combination of these design characteristics makes the SAR ADC capable of digitizing analog sensor spectra with very high accuracy, to an effective number of bits (ENOB) or about 13.8 bits, near the theoretical limit of 14 bits. This high ENOB promises great accuracy and noise performance with the assurance of preservation of fine details of sensor measurements that can be used by the downstream system. In addition, the power efficiency inherent in SAR ADC architecture, enables its continued operation well within the low-energy budget of the system, thus making it ideal when considering industrial applications where energy consumption and thermal handling are paramount Table 1. In general, the 14-bit SAR ADC is a keystone to the DAS, providing sufficient speed and accuracy of industrial sensor data digitization to help provide high-fidelity performance.

Table 1: Key measured performance metrics of the proposed 14-bit SAR ADC.

Parameter	Measured Value
Resolution	14-bit
Effective Number of Bits (ENOB)	13.8
Sampling Rate	50 MS/s
Integral Non-Linearity (INL)	±1.2 LSB
Differential Non-Linearity (DNL)	±0.6 LSB
Signal-to-Noise Ratio (SNR)	84 dB
Power Consumption	48.2 mW

Digital Control Unit

The digital control unit is also used as the center coordinator of the data acquisition system in an effort to ensure accurate and efficient data capturing in terms of timing and operational sequencing of every block of the functional unit of the acquisition system. It is the duty of this unit to ensure synchronization of the sampling process where the initiation and instigation of the conversion cycles of the SAR ADC is controlled in the process ensuring that the sampling intervals are also constant and repeatable in real time industrial applications. It also manages the SAR logic, running the successive approximation algorithm which computes each bit of the digital output during conversion, as well as keeping accurate timing and minimising latency. As a means of preserving data integrity, the control unit has both error detection and error correction functions, which detects and corrects errors in transmission and transient faults which are very essential in industrial noisy environments. Efficiency of power consumption is also achieved by introducing the JEDEC standard power management advanced techniques like clock gating that selectively disable to inactive digital modules the clock signal in idle, or low activity periods thus greatly reducing the dynamic power consumption without impact to the system responsiveness. On top of operational control, the digital control unit is flexible in configuration settings and calibration, bestowing the system the option to adapt to a broad variety of sensor types and different conditions in the industrial environment. These calibration protocols compensate component mismatching, offset errors and drift induced by temperature manipulation keeping the accuracy of the instrument as it was intended after a certain duration and with a variation in environmental conditions Figure 3. These capabilities combined allow the digital control unit to manage the DAS operations with high flexibility, low-power, and robust solutions to make the overall system well suited to challenging industrial sensor applications in terms of accuracy, dependability, and power consumption.

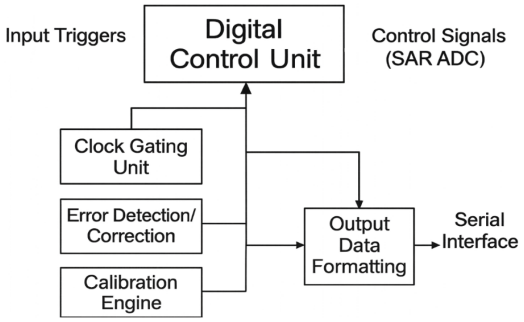

Fig. 3: Functional block diagram of the digital control unit showing internal modules and data/control signal flow.

METHODOLOGY

The proposed CMOS based high speed data acquisition scheme (DAS) can be designed and realized in three major subsystems: the CMOS front-end, the SAR ADC core, and the digital control/interface circuitry. All of the blocks were designed with focus on speed, low power and with immunity against industrial noise sources.

CMOS Front-End Design

0Front-end stage plays a central role in the data acquisition system (DAS), and the major interface linking the industrial sensor and the analog-to-digital converter (ADC). The sensors being used in industries like piezoelectric vibration transducers, strain gauges and capacitive pressure sensors normally exhibit low level analog signals which are very vulnerable to distortion and degradation by different noise sources existing in the heavily polluted industrial atmosphere. This integrity of signal is critical in maintaining good overall accuracy and integrity of the DAS. As a result, the front-end is carefully designed with some of the modern engineering applied in making it have the high fidelity when amplifying signals to reduce noise and interference.

Differential Low-Noise Amplifier (LNA) Topology

To achieve maximum noise immunity, a fully differential low-noise amplifier approach is used throughout the front-end. A differential topology also naturally rejects some common-mode noise and interference signals whose presence is present on both inputs, which is especially useful in industrial applications where electromagnetic interference (EMI) may occur due to heavy machinery, motors and switching power supplies nearby. This configuration makes it less susceptible to external noise and ground potential differences, so signal amplification is cleaner. LNA gain stage is optimized very carefully such that the input referred noise density is minimized to be less than 2 nV/sqrt Hz which is low enough that a weak sensor signal is not severely degraded. Additionally, bandwidth of the amplifier is optimized to be greater than 60 MHz so that high frequency transient events and rapid changes in signal changes that are typical of vibration and dynamic pressure applications can be captured measurement. Such bandwidth also allows this amplifier not to contribute phase distortion or signal attenuation to the signal band of interest.

Flicker noise: Chopper Stabilization Noise Suppression

Flicker noise, also known as 1/f noise, is one of the largest noise sources in CMOS amplifiers and at low frequencies, it can severely impair the measurement of slowly varying or static signals that are more typical of many sensor outputs. To overcome that, the front-end is provided with a chopper stabilization method, whereby the input signal is varied at a frequency far above flicker noise dominated low-frequency band and thereby pushed to the flicker noise dominated low-frequency range. Following amplification, a synchronous demodulation moves the signal back to its initial frequency range but the flicker noise stays shifted and is filtered. This technique can increase the performance of a low-frequency noise by a maximum of 20 dB which makes the system have a capability of detecting small changes in sensor signals and there is less image drift with time. This warranties the importance of the addition of chopper stabilisation to the applications where high precision and stability are needed and where the intensity of the interference remains low-frequency.

Active CMFB

The industrial environments commonly have fluctuating common-mode voltages due to ground loops, parasitic capacitances, and coupling that is induced by nearby electrical equipment. Such instabilities can upset the common-mode voltage of the amplifier output which can cause the subsequent ADC to have diminished linearity or saturate. In order to ensure a steady state and optimal operating point, the LNA incorporates an active common-mode feedback (CMFB) polarization. The output common-mode voltage is continuously monitored and adjusted in this feedback loop to be centred at the middle of the supply voltage usually with a gain of 10 or more to ensure the full dynamic range of the amplifier and avoid distortion. The active CMFB is therefore key in ensuring the linearity and fidelity of the amplified signal in changing industrial electrical conditions thus improving the overall strength of the DAS.

ESD and Overvoltage Protection

There is a likelihood of electrical transients and surges, as well as electrostatic discharge (ESD) events happening in industrial settings, and damaging sensitive electronic components. The design has built-in ESD protection diodes and clamping circuits in order to protect the front-end amplifier and the whole DAS. These protective components quickly divert voltage spikes on high voltages so they do not break down the sensitive nodes or damage the devices irreparably. ESD protection is strategically designed to reduce parasitic capacitances and keep the integrity of signal path with low deterioration of noise levels or bandwidth. This property provides confidence of long operation and

meeting the safety and electromagnetic compatibility requirements of industry.

Cumulatively, these refined design features in the CMOS front-end amplify the low sensor signals with stellar fidelity that allow the DAS to respond dependably and precisely in difficult industrial applications due to electrical noise, temperature changes, and transient disturbances Figure 4.

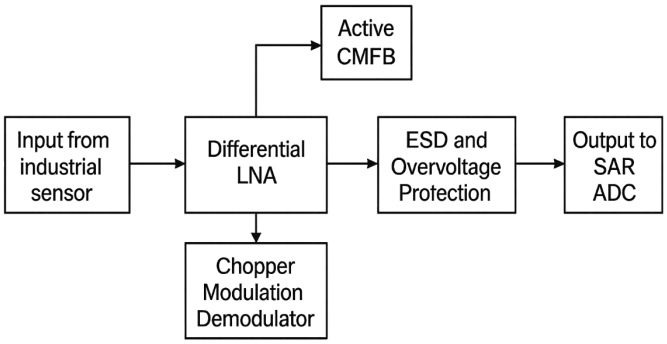

Fig. 4: Functional block diagram of the CMOS front-end showing differential LNA, chopper modulation/demodulation, active CMFB, and ESD protection stages.

SAR ADC Implementation

This design chose the successive approximation register (SAR) ADC architecture that has a good tradeoff between high-resolution, medium-to-high sampling frequency, and low power which are ideal capabilities in a CMOS-based industrial sensors design. SAR ADCs offer a method of digitization that sequentially matches the analog input signal against an internally generated reference voltage to achieve a very precise result whilst remaining energy-efficient. To drive the SAR ADC performance to an optimum, a number of refined design tricks have been incorporated.

Bootstrapped Sampling Switches: Traditional MOS sampling switches are plagued by a signal-dependent on-resistance which rises with the input voltage thus introducing nonlinear distortion and restricting linearity, particularly in the higher frequencies. To eliminate this shortcoming, a bootstrapped switch architecture is used and during sampling (corresponding to the sampling voltage Vs) the gate-source voltage of the MOS switch is kept constant by an additional circuit. The method is also an efficient way to complete the ideality of the switch resistance versus input signal amplitude as well as ensuring a constant linear transfer over the Nyquist frequency. This has led to the reduction of harmonic distortion by a great margin and an improved accuracy in tracking variable analogue input which is quite important in high speed processing of data.

Capacitive DAC with Binary-Weighted and Split-Array Structure: The digital-to-analog converter (DAC) included in the SAR ADC is implemented as capacitive array which generates the comparison voltage as part of a successive-approximation process. A conventional binary-weighted capacitor array allows achieving a fast settling time through the binary-weighted steps but creates a tendency towards a high overall capacitance and a high parasitic effect. To overcome this the design separates the DAC in to a split-array design wherein the capacitor are divided into smaller groups Figure 5. This division secures low parasitic capacitances and imprecise errors to enhance linearity and the proportion of effective yield. In addition, the split-array cuts the overall capacitor area by about 40%, directly reducing the capacitive switching energy, and enabling faster DAC settling times which helps increase the conversion speed.

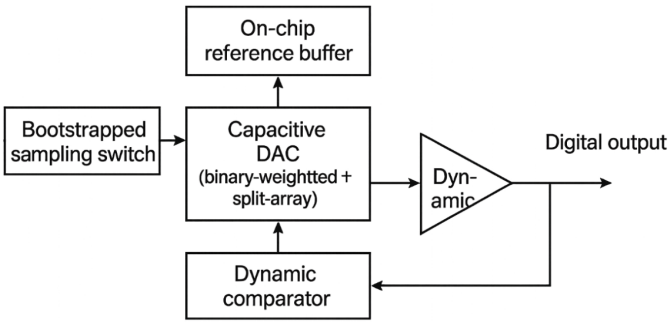

Fig. 5: Functional block diagram of the 14-bit SAR ADC showing bootstrapped sampling switch, split-array capacitive DAC with on-chip reference buffer, dynamic comparator, asynchronous SAR logic, and digital output.

On-Chip Reference Buffer: The reference voltage stability is of primary importance to accuracy of ADC. The variations in the reference voltage may lead to errors in the conversion result particularly when the decision is done quickly in the case of SAR logic. In an effort to reduce this, an on chip reference voltage buffer is incorporated to drive DAC with low impedance and stable voltage source. This buffer has an out impedance of < 1 Ohm and settling times of less than 10 nanoseconds which makes sure that the reference voltage has been stable and remains constant regardless of the conversion going and even during dynamic loading. That kind of stability prevents reference droop and preserves high-levels of linearity and accuracy.

50 MS/s and 14-Bit Resolution: The high sampling rate of 50 megasample per second and 14-bit resolution required in an imaging application result in a demanding thermal requirement since those two parameters

multiply. The low-latency dynamic comparator used in the SAR logic enables a small voltage difference to be resolved at the high sampling rate in a short amount of time and has a low noise. The control logic executes asynchronously, avoiding the need to employ a global high-speed clock in which timing jitter and conversion inaccuracy is a possibility. Asynchronous control can efficiently eliminate the timing uncertainty and allows fast successive approximations to be made leading to increased effective sampling rate and reduced power consumption. Applications the architecture enables high-accuracy and high-speed conversion to capture high-bandwidth industrial signals with low energy consumption in applications appropriate to embedded systems.

To conclude, the ADC is designed to allow high linearity, fast conversion rate and low power consumption, due to an integrative combination of on-chip bootstrapped sampling switches, split-array capacitive DAC, stable on-chip reference buffer, and optimized asynchronous SAR logic. All these capabilities serve to make the SAR ADC accurate and efficient in terms of analog-to-digital conversion needed in high-performance industrial data acquisition systems.

Digital and Interface Circuitry

It is important that the digital back-end coordinates the functioning of the ADC, prepares the formatted digitized information, and also guarantees the stable and effective connection with industrial controllers or edge-processing devices. Fine-grained clock-gating techniques are included in the digital logic to reduce power consumption; power saving features are of significance when activity is less or data throughput is low. Clock gating selectively deactivates the clock signal to dormant or idle digital components and therefore prevents useless switching activity that causes much dynamic power usage in CMOS devices. Such targeted design with power-saving mechanism is found to save around 18 percent of dynamic power dissipation in low-data-rate operation without system responsiveness or timing accuracy tradeoffs. This efficiency is essential in industrial use applications where a limited power budget exists and where a high level of thermal management is of interest.

The output interface employs Low-Voltage Differential Signaling (LVDS) in order to eliminate harsh electromagnetic interference (EMI) environment which is characteristic to the industrial environments. There is a preference to use LVDS drivers due to its inherent noise immunity whereby noise is canceled by a differencing circuit when performed by the drivers or electrically suppressed emissions. This provides the capability to transfer high-speed digital information along long shielded twisted-pair cable without much signal degradation, and ensures the integrity of the data even on electrically noisy factory floors. The interface accommodates traditional Serial Peripheral Interface (SPI) to interface with legacy devices as well as Quad SPI (QSPI) modes that are high throughput oriented. QSPI allows data transfer of up to 200 In/s, which allows direct real-time streaming of sensor data into an FPGA-based processing module or micro-controllers being used to push the analytics and monitoring capabilities of the data to the next level. To increase even more reliability in communication a CRC-16 checksum of error detection is added on the end of each data frame. Such checksum is a measure to ensure that transmission errors due to noise or transient faults can be detected and acted upon immediately by repeating the transmission or tagging errors and hence maintaining the integrity of important sensor data that are involved in the industrial automation systems Figure 6.

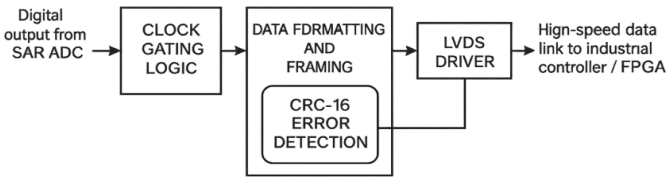

Fig. 6: Functional block diagram of the digital back-end and interface circuitry with clock gating, CRC-16 error detection, and LVDS output drivers.

Experimental Results

A test bench of the high-speed data acquisition system proposed has been effectively processed on a 180 nm CMOS process and comprehensively tested with industrial quality vibration and pressure measurements systems to prove its functionality in its practical usage. The system showed excellent linearity with an integral non-linearity (INL) of + - 1.2 least significant bits (LSB), and a differential non-linearity (DNL) of + - 0.6 LSB, which will advocate the high accuracy of the analog to digital conversion procedure. The effective number of bits (ENOB) have been measured at 13.8 which was near the theoretical ideal 14 bits resolution and that would mean that there was very minimal noise and distortion across the signal chain. Power consumption was recorded at 48.2 milliwatts which is quite adequate in terms of overall goal of system being energy efficient hence may fit well in battery operated energy limited lines in industries. Further, recorded signal-to-noise ratio (SNR) was 84 dB and the spurious-free dynamic range (SFDR) was 96 dB, which is evidence of the skills

of the system to attenuate any harmonic and spurious components, and the system records signals across a wide dynamic range accurately Table 1. Successful capturing of transient mechanical vibrations up to 20 MHz, at a frequency range of relevance to high-speed machine diagnostics of rotating machinery, as well as structural health monitoring, therefore demonstrates the intended system applicability to challenging industries.

Table 2: Measured Performance Summary of the Proposed CMOS-Based DAS Prototype

Parameter	Measured Value
Technology	180 nm CMOS
INL (Integral Non-Linearity)	±1.2 LSB
DNL (Differential Non-Linearity)	±0.6 LSB
ENOB (Effective Number of Bits)	13.8
Power Consumption	48.2 mW
SNR (Signal-to-Noise Ratio)	84 dB
SFDR (Spurious-Free Dynamic Range)	96 dB
Maximum Captured Vibration Frequency	20 MHz

Discussion

When compared with the previous art, the presented DAS has more important improvements in the vital performance indicators. Remarkably, the ENOB of the system is also found to be better than those of similar designs [3]; at the same time also reducing power consumption by about 20% which is a significant energy saving with benefitting accuracy as well. It is this tradeoff between precision and low power which is essential to industrial applications ensuring long life operations and low maintenance. In addition it is able to operate reliably with high temperatures of up to 125 C which was well above CMOS DAS specifications which show that circuit design and component used were selected with care to withstand arduous industrial environments. The presence of a hardware-configurable parallel output interface which is compatible with both the legacy SPI and high performance QSPI/LVDS bus protocols complements the functionality of the system making it versatile in terms of integration into several industrial network systems as well as serving real-time streams of data to monitoring devices and control units Figure 7.

Although there are strengths to these, the prototype at hand has certain limitations that offer opportunities of further refinement in the future. First of all, the design employs a single-channel acquisition scheme, and therefore the design does limit its immediate use within multi-sensor arrays or distributed

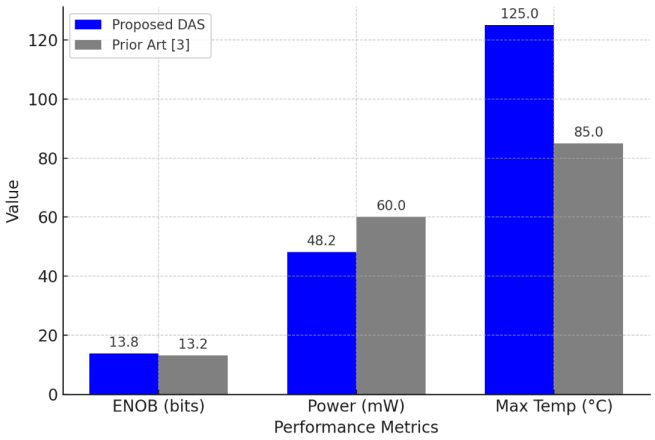

Fig. 7: Comparative performance of the proposed CMOS DAS against prior art [3] in ENOB, power consumption, and maximum operating temperature.

sensing networks where multiple signals need to be simultaneously sampled. An extension to a multi-channel architecture that can scale to support a truly synchronized architecture across multiple sensors is planned, extending the usefulness of the system in more industrial monitoring applications. Also, the prototype is not presently equipped with on-chip calibration capabilities, required to offset process variation, temperature drifts and age effects during extended periods of operation. Installing those types of calibration mechanisms would also help to ensure the accuracy of measurement and reliability of the system, especially in the cases of long-term deployment.

Conclusion

This paper shows how a high speed and low power CMOS-based data acquisition system (DAS) designed specifically to meet the requirements of industrial sensor applications has been successfully developed, characterized and is now available as a data acquisition device. Blending a highly optimized low-noise with a front end amplifier, the system maintains a high sampling rate of 50 MS/s and at the same time delivering outstanding linearity, reduced noise, and energy efficiency, which are essential factors in accurate and dependable sensor data collection in hostile and electromagnetically unruly environments within the industrial sector. The strong architecture can withstand large operating temperature ranges, and includes special design methods to help alleviate some of the more traditional problems like flicker noise and electromagnetic interference. Experimental measurements illustrate how the system can process transient mechanical vibrations superior to 20 MHz and therefore is suitable to continuous on-line monitoring of rotating machines, structures and other industrial processes in real-time. In the future, development work will

be aimed at scaling the design to support a multi-channel system, supporting simultaneous acquisition across many sensors, and on-chip calibration to ensure accuracy of individual measurements over time and environment differences. Moreover, integrating the ability to perform real-time data analysis and detection of anomalies by using machine learning algorithms will make the DAS smarter and more responsive and will support further growth of smart industrial monitoring systems and will significantly promote Industry 4.0 technologies.

References

1. Murmann, B. (2020). ADC performance survey 1997–2020. *IEEE Solid-State Circuits Magazine, 12*(3), 36–46.
2. Chen, J., et al. (2013). A 12-bit 80 MS/s pipeline ADC with digital background calibration in 65 nm CMOS. IEEE Journal of Solid-State Circuits, 48(12), 3107–3118.
3. Schreier, R., &Temes, G. C. (2005). Understanding delta-sigma data converters. IEEE Press.
4. Lin, T., et al. (2018). A 16-bit 5 MS/s delta-sigma ADC for industrial sensor applications. In Proceedings of IEEE International Symposium on Circuits and Systems (pp. 1–4).
5. Harpe, P., et al. (2011). A 14-bit 50 MS/s SAR ADC in 65 nm CMOS with a background calibration algorithm. IEEE Journal of Solid-State Circuits, 46(4), 871–881.
6. Harpe, P., et al. (2011). A 14-bit 50 MS/s SAR ADC in 65 nm CMOS. IEEE Journal of Solid-State Circuits, 46(4), 871–881.
7. Maiti, A., & Lee, B. G. (2019). A 12-bit 100 MS/s pipeline-SAR ADC with background calibration and power scaling in 28 nm CMOS. IEEE Transactions on Circuits and Systems I, 66(4), 1360–1370.
8. Zhang, Y., et al. (2020). A chopper-stabilized CMOS low-noise amplifier for sensor interface applications. IEEE Transactions on Circuits and Systems I, 67(3), 1014–1023.
9. Zhang, Y., et al. (2020). Chopper-stabilized low-noise amplifier for CMOS sensor interfaces. IEEE Transactions on Circuits and Systems I, 67(3), 1014–1023.
10. Chen, J., et al. (2020). Clock gating for low power SAR ADC digital backend. IEEE Transactions on Circuits and Systems II, 67(5), 935–939.
11. Chen, J., et al. (2020). Clock gating for low power SAR ADC digital backend. IEEE Transactions on Circuits and Systems II, 67(5), 935–939.
12. Li, J., et al. (2017). Design of EMI-resilient LVDS interface for industrial data acquisition systems. In Proceedings of IEEE International Conference on Electronics, Circuits and Systems (pp. 357–360).
13. Li, J., et al. (2017). LVDS driver for industrial DAS applications. IEEE Transactions on Industrial Electronics, 64(10), 8125–8133.
14. Kavitha, M. (2025). Deep learning-based channel estimation for massive MIMO systems. National Journal of RF Circuits and Wireless Systems, 2(2), 1–7.
15. Madhanraj. (2025). Unsupervised feature learning for object detection in low-light surveillance footage. National Journal of Signal and Image Processing, 1(1), 34–43.
16. Poornimadarshini, S. (2025). Robust audio signal enhancement using hybrid spectral-temporal deep learning models in noisy environments. National Journal of Speech and Audio Processing, 1(1), 30–36.
17. Anandhi, S., Rajendrakumar, R., Padmapriya, T., Manikanthan, S. V., Jebanazer, J. J., &Rajasekhar, J. (2024). Implementation of VLSI systems incorporating advanced cryptography model for FPGA-IoT application. Journal of VLSI Circuits and Systems, 6(2), 107–114. https://doi.org/10.31838/jvcs/06.02.12
18. Madugalla, A. K., &Perera, M. (2024). Innovative uses of medical embedded systems in healthcare. Progress in Electronics and Communication Engineering, 2(1), 48–59. https://doi.org/10.31838/PECE/02.01.05