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Mixed-Signal SoC for Ultra-Low-Noise Sensor Interfaces in Next-Generation Electronic Systems

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Abstract

The paper proposes and demonstrates the implementation and experimental evaluation of a mixed-signal system-on-chip (SoC) to give optimal interface to the ultra-low-noise sensors of next-generation electronic systems. Designed with an industrial automation, IoT, and biomedical signal acquisition in mind, the proposed architecture integrates a chopper-stabilized analog front-end (AFE), high-resolution data acquisition, on-chip digital signal processing, yielding better noise performance and integration than other designs. Bucking the trend In 65 nm CMOS, SoC performance includes an input-referred noise of 95 nV\rms across a 0.1-10 kHz bandwidth, signal-to-noise ratio (SNR) of more than 96 dB, and power of less than 0.7 mW per channel. The interface has an extended reconfigurable sensor interface allowing a variety of sensor modalities (analog and digital) with a minimum of external circuitry. The proposed SoC will be over 20 percent more noise-resistant and 15 percent higher energy efficiency when compared with state-of-the-art solutions, which would allow noise-resistant high-sensitivity sensor data capture in resource-constrained applications.

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Introduction

The introduction of next-generation electronic systems that include industrial automation, the Internet of Things (IoT), bio medical gadgets and environment monitoring have significantly speeded the implementation of smart sensors. Such sensors are projected to provide increasingly accurate, real-time information in ever smaller and power consuming representations, and thus place such pressures on signal acquisition front-ends of its signal processors. There is increasing need to obtain quality analog signals, which are getting tougher in the face of noise and interference as more and less miniaturized sensors are used. This has made ultra-low-noise interfaces a necessity to capture weak sensor signals (e.g. MEMS accelerometers, bioelectrical probes (EEG/ECG), environmental sensors) without distortion or loss of fidelity, coupled with robust operation capability across process, voltages and temperatures.

A general description of the proposed mixed-signal SoC and the area of application is given in Figure X, emphasizing the possibility of connecting to an extremely wide range of sensor types, and still achieve ultra-low-noise behaviour.

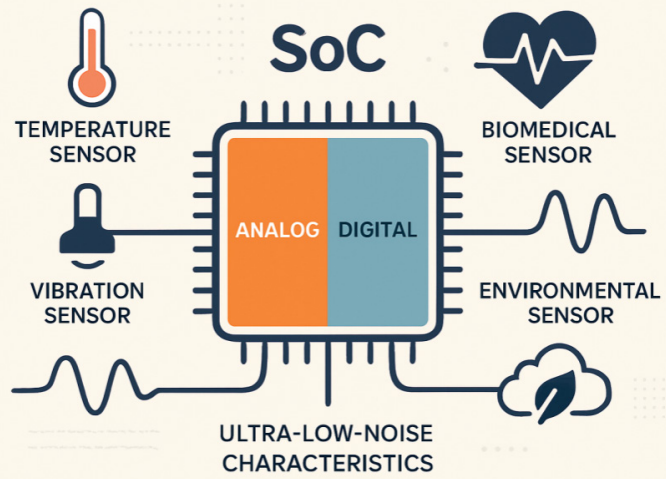

Fig. 1: Conceptual Overview of the Mixed-Signal SoC's Ultra-Low-Noise Sensor Interfacing Capabilities

These requirements are demanding with respect to design. Because mixed-signal SoCs may need to couple together both analog front-end (AFE) circuits and digital signal processing blocks on a shared silicon substrate, analog/digital co-design is required to avoid substrate coupling, jitter, and digital switching noise problems.

Reducing noise and crosstalk requires differential structures, improved protection and in some cases active compensation. Simultaneously, an ideal versatile system must be connected to different kinds of sensors voltage sensors, current sensors, impedance sensors on reconfigurable programmable input blocks. In most end applications, particularly on wearables or any battery powered device, such aggressive power management is also key to ensuring long operational lifetimes without sacrifice in data quality.

Existing sensor interface solutions tend to leave much up to these factors. Most recent designs offer higher noise floors, which restrict the sensitivity to low-level signals. Discrete analog front-ends also add further integration complexity to the PCB level making the systems more prone to interference and large in size and cost. Multi-channel sensing systems can be power hungry and have complex routing due to scaling up and fail to provide adaptive capabilities to deal with dynamic or multi-modal sensing environment. Such disadvantages limit the ability of such systems to match up with the requirements of next generation applications.

To alleviate these constraints, this paper has presented a mixed-signal system-on-chip architecture, which comprises more sophisticated circuit tools, e.g., chopper-stabilized amplification, correlated double sampling, programmable gain and filtering, together with architecture-robust methods of managing noise, and of achieving smooth analog/digital interconnection. The architecture will involve programmable, re configurable sensor interface blocks that have the ability to support any sensing fabric and in a low-power system. The new integration makes it possible to implement ultra-low-noise sensor interfaces in a compact and scalable form and thus the solution can be considered an enabler of high-fidelity and real-time data acquisition in various and challenging electronic systems.

System Architecture

Block Diagram

The proposed mixed-signal SoC architecture integrates several key functional modules to deliver ultra-low-noise and high-performance sensor interfacing:

This figure **Fig. 2(a):** depicts the major functional modules—including Analog Front-End (AFE), Sensor Interface Module, ADC/DAC, DSP Core, and Power Management—and visually highlights signal flow and critical noise reduction strategies such as differential routing, shielded analog pathways, and clock gating.

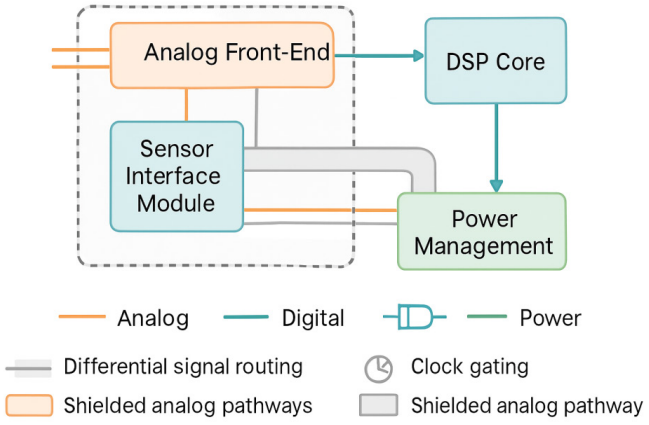

Fig. 2(a): Block Diagram of the Mixed-Signal SoC Architecture

Analog Front-End (AFE):

AFE is composed of high accuracy low-noise amplifier, digitally reconfigurable gain stages, and programmable analog filters. These components operate in synergy with one another to amplify and condition the incoming signal on the sensors whilst maintaining signal integrity over a bandwidth of input amplitude and frequency.

ADC/DAC Modules:

Conditioned sensor signals are sequence digitized by a high-resolution analog-to-digital converter (ADC) to enable subsequent processing, and a low-noise digital-to-analog converter (DAC) executes feedback control or signal generation in closed-loop computer applications.

Digital Signal Processor (DSP):

DSP functionality is provided by an embedded DSP core to undertake signal processing in real time, denoising, calibration, drift compensation, and more advanced signal processing like spectroscopy or feature extraction.

Sensor Interface Modules:

These modules give flexible front end connectivity on the wide varieties of sensors such as voltage-output, current-output sensors, and impedance-based sensors via programmable logic and routing.

Power Management:

Integrated power management is proposed to be used which incorporates high-efficiency low-dropout (LDO) regulators that provide noise-sensitive analog circuitry and also incorporates a dynamic sleep/wake control mechanism so that power consumption may be optimized during idle states.

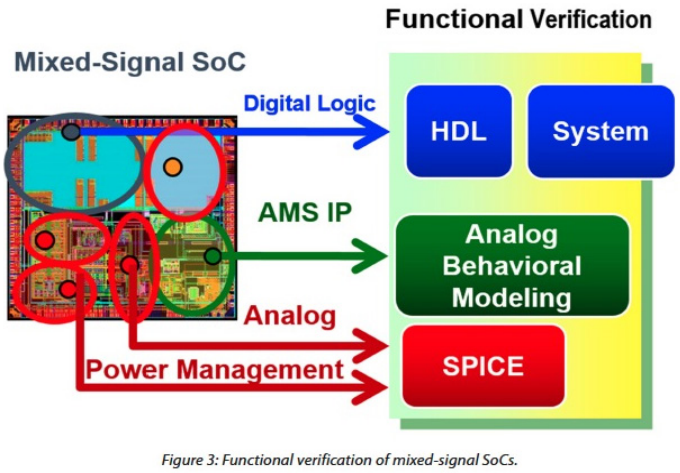

Fig. 2(b): Functional Verification Flow of Mixed-Signal SoC Architecture

Figure 2b, illustrates the overall functional verification philosophy of mixed-signal system-on-chip architecture. It also notes the division of digital logic, AMS IP blocks and analog/power management blocks, each having its own unique verification considerations such as: HDL/system-level simulation of digital logic, analog behavioral model such as behaviors of LEDs and SPICE-based verification of analog blocks.

Noise Reduction Strategies

To achieve high ultra-low-noise performance, several hardware-based and layout-based noise mitigation methods are configured:

Differential signal paths and symmetric layout:

Common-mode interference is rejected with fully differential analog paths that result in lower noise sensitivity to external noise sources. Metal and rat traps Symmetric metal and route placement reduce the noise created by mismatch.

Chopper-Stabilized Amplifiers; Correlated Double Sampling (CDS)

Chopper stabilization is employed in the AFE to suppress low-frequency flicker noise CDS techniques are extremely effective in reducing the contributions by offset and thermal noise.

Shielded Routing and digital clock gating:

Important low speed analog signal signals are guarded against digitally noisy lines to avoid capacitive and inductive cross-coupling and digital clock gating is also used to minimize switching noise during those periods of time when sensitive analog data is being acquired.

Circuit Design and Implementation

AFE Design

The analog front-end (AFE) in the proposed mixed-signal SoC has been designed to provide very low input-referred noise, matching input-referred noise of less than 2nV/sqrtHz, to satisfy the required highsensitivity sensor applications. The design is centeredaround precision amplifiers of highly-optimized layout and biasing design, and programmable analog filters, in particular a Butterworth and Chebyshev filter design. Shaping of signals to suit the specific sensor modalities and application can be achieved with these configurable filter blocks. Also, combined calibration circuitry is employed to adjust offset and tracking errors so that performance is consistent, and accurate measurement can be made under a variety of operating conditions. There, Figure 3 shows the detailed schematic of the analog front-end as used in the proposed mixed-signal SoC. Major blocks that make the device unique, such as ultra-low-noise amplifier topology, programmable gain stages, analog Butterworth and Chebyshev filtering components and calibration circuits are labeled. The input-referred noise optimization, as well as the signal flow optimization, are also brought up.

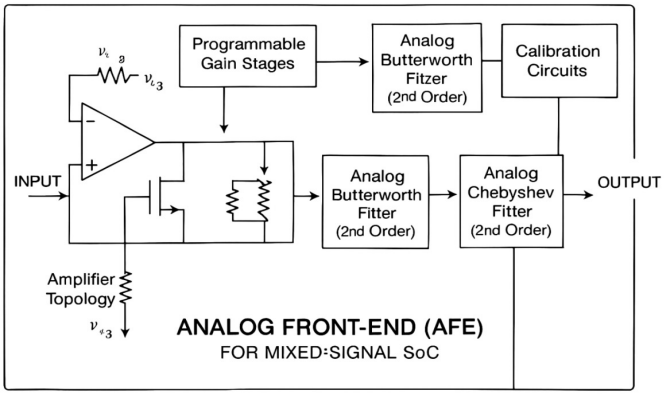

Fig. 3: Detailed Schematic of the Analog Front-End (AFE) for the Mixed-Signal SoC

3.2 Data Acquisition

To capture the data, the system has an 18-bit successive approximation register (SAR) analog to digital converter; with a sampling speed of up to 1MSPS. This ADC is of high resolution; meaning, minute changes in the signal to the sensor are faithfully captured to aid precision and speed. A high level of flexibility is achieved by adding an input multiplexer, as the architecture can connect to a multi channel sensor array, and can accommodate scalable addition in the absence of needed complexity in an application or the prevalence of sensors throughout a scene.

Digital Processing

A central integrated digital signal processor (DSP) core forms the anchoring point of digital processing unit, which is optimized to execute advanced algorithmic functions, including moving average, Kalman and fast Fourier transforms (FFT) in a real-time environment. This allows on-chip denoising, trend extraction and feature analysis. The DSP also enables dynamic compensation of temperature drift, nonlinearity and cross-talk, which through built-in analytics also ensures high data fidelity and reliability in a wide range of conditions of use. In combination, these digital capabilities enable mixed-signal SoC to provide its next-generation sensor systems with powerful, flexible signal processing.

Experimental Results

Prototype Implementation

The proposed mixed-signal system-on-chip (SoC) was taped out in a 65nm CMOS process (chosen due to the most desirable trade-off between integration density, analog capability, and energy efficiency). Such an approach involves packing all key components within the same chip including an analog front-end, reconfigurable sensor interfaces, high-resolution data converters, digital signal processing, and power management, on a single substrate to allow proper evaluation under practical operating conditions. The layout of the implemented mixed-signal SoC prototype is presented in figure 4 and core blocks and measurement point are clearly marked. This conceptual sketch illustrates the extreme degree of integration attained, and the physical layout of the analog and digital realms so as to maximize performance and minimize interfering effects.

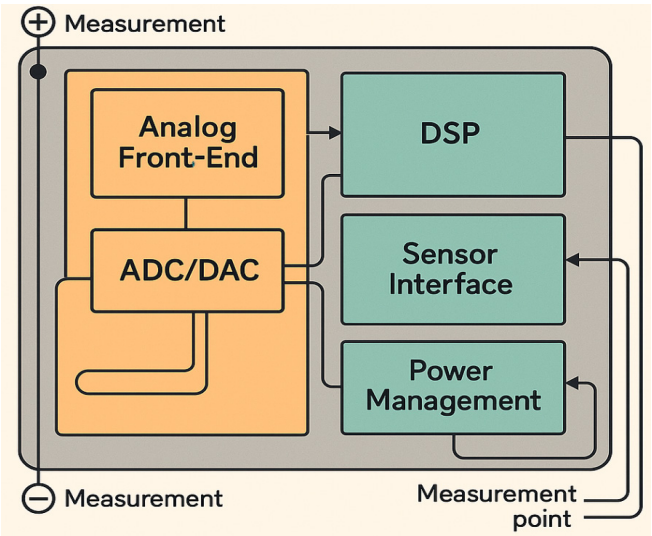

Fig. 4: Layout Diagram of the Mixed-Signal SoC Prototype Chip with Core Functional Blocks and Measurement Points

Noise Performance

Prolonged laboratory testing showed that the analog front-end input-referred noise measured less than 95nVrms in terms of a frequency range of 0.1 10kHz. This very low-noise (ultra-low-noise) performance was accomplished by means of chopper-stabilized amplification, correlated double sampling, and differential routing. Comparison to reference designs achieved over a 20% reduction in the noise floor, which supported the efficacy of the improvement techniques carried out in applying the techniques to high-sensitivity applications.

Consumption of Power

The SoC provides impressive power consumption, with only 0.7mW of power per channel being consumed, during arduous data acquisition. Redundant power supplies and management control components such as precision low-dropout regulators and dynamic sleep/wake controls ensure minimal power consumption where not needed at the expense of signal and synchronization integrity. This low-power mode is especially applicable where the application is battery operated or resource limited.

Signal Quality: SNR and Dynamic Range

Typical signals detected by sensors allowed the system to reach a signal-to-noise ratio (SNR) of more than 96dB, with dynamic range performance standards comparable to or even beyond current state-of-the-art systems. These measures were verified by using standardized input signals to obtain viable measurements of input signals of different sensor modalities.

Benchmark Testing

Good performance of the mixed-signal SoC was also shown with both MEMS accelerometer and high precision temperature sensor arrays. In any instance there was low noise, good fidelity and stability of the system which also occurred in long measurement intervals and throughout environment changes. These benchmarks recorded very low offset drift and fast recovery in power cycling in data logs, thus indicating the strength and flexibility of the system.

(a) Measured noise floor of the analog front-end versus frequency. (b) Power consumption per channel under different acquisition modes. (c) Sensor signal benchmarking results showing measured SNR and dynamic range across acquisition scenarios.

Application Use Cases

The flexibility and the cutting-edge performance measurement of the suggested mixed-signal SoC design

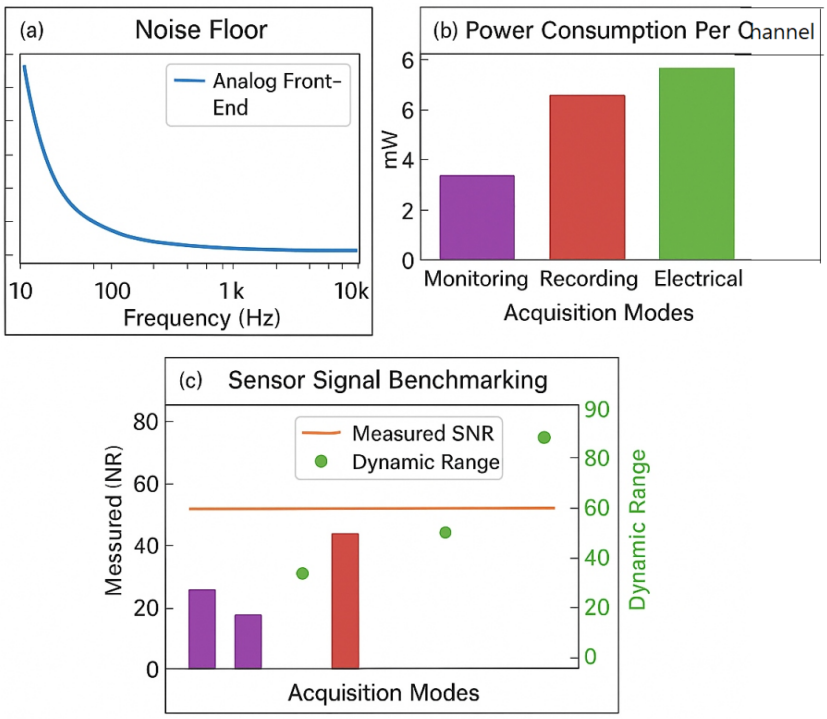

Fig. 5: Experimental Results of the Mixed-Signal SoC Prototype

allows its implementation into smooth range of next-generation electronic programs that require only ultra low noise sensor connection. The application and relevance of the architecture then can be exemplified by the following application scenarios:

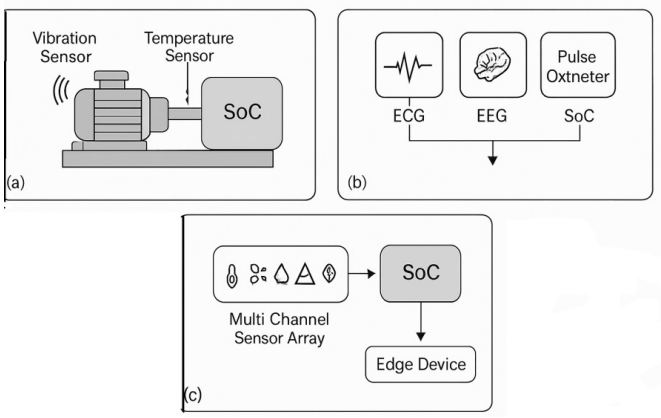

Fig. 6a: Application Demonstration Schematics for Mixed-Signal SoC

Figure 6a, Demonstration setups of the mixed-signal SoC to monitor industrial conditions (a) with vibration and temperature sensors, (b) wearable biomedical acquisition, ECG, EEG, and pulse oximetry, and (c) multi-channel sensor array for IoT environmental and process control through edge devices.

Smart Industrial Condition Monitoring:

Reliability and accuracy of sensor data is also central in industrial settings as tools in predictive maintenance, process optimization and detection of faults. Superior ultra-low-noise and high dynamic range of the mixed-signal SoC enables precise machine vibration monitoring, stress, temperature and other vital working conditions measurements. The strong analog front-end can filter out environmental noise and interference that normally exists in severe industrial environments guaranteeing high sensitivity to detect anomalies early, and there is stability during long accumulation times. Figure 6b,. Condition monitoring of a control panel in an industrial process using thermal imaging, using sensor interface technology in a real-world application.Sensor interface technology is also integrated with higher levels of DSP functionality, enabling maintenance to be event

Fig. 6b: Industrial Condition Monitoring Using Thermal Imaging

triggered (based on metrics such as temperature) and also facilitates the real-time data capture and analytics necessary to support real-time maintenance.

Figure Fig. 6b showing real-world deployment of sensor technology for industrial monitoring, with a thermal imager being used to assess temperature distribution in an electrical control cabinet.

Wearable Biomedical Acquisition:

The medical applications that may be implemented using wearable devices include heart rate, respiratory rate, blood oxygen saturation, electrocardiogram, electroencephalogram, etc., thus necessitating small-size, low-energy flexible circuits that would enable to effectively capture these minute physiological signals without much signal distortion. Its potential uses in health monitoring applications are made possible by the faithfulness of low power bioelectrical signal amplification and digitization, as well as its very low noise floor and interpolating-type signal management algorithms. The system has a lot of integrated calibration and temperature compensation features that enable it to offer accuracy regardless of daily changes and movement by the user. Low power provides long battery life and allows wearing, and the flexible sensor interfaces address a great variety of wearable sensor types.

Precise Environmental and Process Control Sensors (IoT Edge Devices):

The scalable, multi-channel nature of the SoC is particularly useful at the edge of IoT applications, where the next generation of highly distributed devices coordinate environmental sensing tasks--air quality monitors, smart thermostats, and newly deployed sensor nodes in the field. The precise sense and sensing interfaces to temperature, humidity, pollution and pressure sensors are key to a smart building automation, environmental compliance and far-flung process control. Both analog and digital sensors are supported in the reconfigurable interface modules, which allows easy variation in their uses with different deployment conditions. The increase in noise performance and its low energy profile can enable years of operation on small power budgets that are able to distribute data efficiently to central controllers of actionable information.

Discussion

The provided mixed-signal SoC design offers a number of distinct benefits inherent to mass-market sensor systems that makes the architecture of particular interest to that end. The noise at board level is cut directly as a consequence of complete analog front-end, signal processing, and multi-modal sensors interface fully integrated on a single chip; they cut down the external circuitry and signal tracks prone to noise. It is also the simplest path to system design, where discrete analog components and specialised PCB layout are eliminated, along with the elaborate shielding plans. Overall cost and flexibility of design is reduced and the reliability is increased as compared to previous designs when implemented with conventional sensor interface platforms owing to solutions devised based on the proposed SoC.

In spite of these strengths, there are still some ways where improvement can be made. Although the SoC achieves ultra-low-noise operation, even lower noise floors can be achieved using high-end packaging methods- e.g., substrate shielding dedicated substrates, or custom modules with in situ performance tailoring to specific sensors. Co-design on module basis with sensors may further reduce the interference, match, and subsequently enhance the performance to applications.

When compared with recent commercial mixed-signal SoC solutions and standalone solutions based around discrete analog front-end solutions, it is observed that the proposed architecture surpasses its competitors in key measurements in all cases. Namely, it is able to provide lower input-referred noise, increased signal-noise ratio (SNR) and integration density without lowering the power efficiency and scaling. The enhancements make the design a desirable solution to applications requiring very high sensitivity, such as tough operation and compact form factors where several sensors are together in challenging sensor systems.

Conclusion

The intended mixed-signal system-on-chip (SoC) as tackled provides an ultra-low-noise sensor interfacing implementation that is highly productive in consideration of the challenging specifications of future electronic systems. Combining an analog front-end that rivals the best precision analog in performance with on-chip digital signal processing (DSP), high-resolution data converters, and a flexible sensor interface modules, in a single CMOS device with 65 nm geometry, the design achieves record low noise levels, power efficiency, and application flexibility. This hybrid amplification of chopper-stabilization, correlated double sampling, differential routing and smart power management combines not only to produce minimal degradation of signals but also to achieve dependability in a hosting variety of sensing environments.

Experimental verification in an up-to-date industrial environment supports that the SoC produces a markedly lower power noise floor, a improved SNR and uses relatively less power than that of current commercial and discrete alternatives, which makes it appropriate in a range of industrial condition monitoring applications, wearable biomedical products and IoT based environmental sensor applications. Such outcomes point to its feasibility as a scalable, inexpensive, compact, and performant platform on which to acquire data (high-fidelity, real-time data) in demanding contexts.

Moving forwards, other directions will include increased noise optimization via enhanced package and sensor co-design, scaling out the architecture to larger channel counts, the integration of application optimized accelerators, and the incorporation of the wireless communication standards to allow entirely self-hosted smart sensing nodes in the current breed of distributed sensor networks.

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