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RESEARCH ARTICLE

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Design and Performance Analysis of a Compact Wideband RF Front-End for 5G and Beyond Wireless Systems

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Abstract

Combined with the growing pace of the fifth-generation (5G) and even beyond-5G wireless systems the need of compact, wideband, and energy-efficient radio-frequency (RF) front-end architecture with the ability to support multi-standard and reconfigurable transceivers has risen. This paper describes and discusses a small-scale wideband RF front-end that is aimed at supporting 5G and other sub-6 GHz wireless technologies. This proposed architecture has incorporated a wideband low noise amplifier (LNA) and RF switch to allow broadband impedance matching, low noise performance, and an improved linearity using a smaller silicon area. Front-end is at standard CMOS and is optimised to operate over wideband on the order of careful matching network design, layout-wise considerations. The RF front-end proposed allows continuous operation at 3 -8 GHz, encompassing important 5G bands that are sub-6 GHz, with stable gain, low input reflection, and power consumption. A thorough performance assessment is realised at post-layout simulations, that is, S-parameter analysis, noise figure, linearity measurements, power efficiency. Influence of structure of parasitic effects and layout on overall RF performance is also discussed. The comparative analysis against recently reported RF front-end design proves that the proposed solution has a better trade-off between bandwidth, noise performance, linearity and chip area. These findings demonstrate that the suggested compact wideband RF front-end can be effectively used in the next generation multi-band and versatile wireless transceiver based on 5G and more wireless systems.

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Introduction

This is because, fifth-generation (5G) wireless communication systems and newer beyond-5G systems are intended to accommodate high data rate, ultra-low latency and high numbers of devices in application conditions of increased mobile broadband, Internet of Things (IoT), and software-defined radio systems. These needs have driven the need to have flexible and wideband radio-frequency (RF) front-end architectures that can be configured to work with various frequency bands while not needing high power consumption and low form factors.[1, 2] The frequency range of the 5G New Radio (NR) RF front-ends within sub-6 GHz (FR1) spectrum (high frequency range) requires the

wide instantaneous bandwidths to facilitate carrier aggregation, dynamic spectrum management, and multi-standard configuration. Nevertheless, much of the current RF front-end architectures are still narrowband frequency bands or single bands, and lack the flexibility to change with current wireless standards of 5G and beyond.[3, 4] Although a number of wideband low-noise amplifier (LNA) designs have been implemented, many of these designs do not consider front-end-level integration, so their implementation does not translate into significantly reduced area, lowering the overall receiver sensitivity, or worse noise and linearity characteristics when incorporating RF switching stages.[5, 6] Although an LNA design has been reported in a number of different cases, many of the reported cases simply consider network-level design in isolation, and not the overall implementation, leading to greater area, reduced sensitivity of the receiver, or poorer noise and linearity consider These elements include the LNA and RF switch, which have great impact on bandwidth, noise figure and linearity especially in wide band receivers. The combination of the mentioned blocks into a small-scale layout and maintaining broadband impedance comparable with and stable gain is a challenging design issue because of the natural trade-offs between noise performance, gain flatness, linearity, and silicon area.[7]

The paper is aimed at overcoming these challenges by suggesting a miniaturised wideband RF front-end architecture based on a broadband LNA and an RF switch tailored to sub-6 GHz 5G and beyond wireless networks. The important works of this work can be summed as follows:

- 3-8 GHz wideband RF front-end design, including the most important 5G FR1 applications and new applications in multi-band wireless.
- Circuit-level analysis A broadband LNA and RF switch with a wide impairance matching, low noise figure, and enhanced linearity Circuit-level analysis An analysis of a broadband LNA and RF switch that achieves a wide impairance matching, low noise, and better linearity.
- CMOS implementation and extensive performance Analysis including layout-aware implementation and end-to-end performance analysis showing competitive trade-off between bandwidth, noise performance, linearity and area with the latest state of the-art designs.

Related Work

The wideband RF front-end design has been paid much attention in recent years because of the requirement of multi-standard and reconfigurable transceivers in wireless communications. Most of the literature has been dedicated to wideband low-noise amplifier (LNA) designs, such as common-gate (CG), resistive-feedback (RFB), and noise-cancelling (NC) designs, which have an intrinsic input-impedance characteristic of wideband input. CG-based LNAs have wideband matching with single input networks, but normally have poor noise figure and low gain. The resistive-feedback LNAs enhance the input matching and spacing but generally consume a lot more power and noisier tools because of the resistor which is used as a feedback. Some of these limitations can be reduced using noise-canceling architectures but at the cost of more circuitry, in both design complexity and silicon area. In addition to individual LNAs, a number of studies have explored integrated RF front-end systems that have used LNAs together with RF switches, tunable matching networks or filtering stages to enable the multi-band operation.[9] Though these designs improve integration on system-level, most of the reported designs are focused on small frequency bands or are designed to optimise on a single standard, and may not be applicable to wideband sub-6 GHz 5G applications. Moreover, when RF switches are incorporated, extra effects of insertion loss and parasitic can arise and this can substantially ruin noise figure and linearity unless designed in with the LNA.[10] Current wideband RF front-end designs based on sub-6 GHz 5G systems have shown promising performance gains and bandwidth performance although often require complex matching networks or external passive components or large on-chip inductances into the circuit, increasing chip area and decreasing scale.[11] The optimal strike of wide bandwidth, low noise figure, high linearity, and compact area is one of the challenges that persist been RF front-end designs as it will be summarised in Table I.

Unlike the existing work, the proposed RF front-end focuses on on-chip implementation of a wideband LNA and RF switch in a compact on-chip format and joint matching and layout-aware design as a way of achieving broadband functionality and competitive performance indicators that can be implemented into 5G and more wireless system.

Proposed RF Front-End Architecture

The build to be proposed is an RF front-end architecture, which includes a low-noise amplifier (LNA) of wideband capability and then an RF switch stage (as illustrated in Fig. 1). This is an architectural decision driven by the necessity to attain the broadband signal amplification capacity and also allow the flexible signal routing between sub-6 GHz 5G and beyond wireless systems. The cascade

of an LNA and RF switch is a basic receiver front-end structure that is ideal when time division duplex (TDD), antenna selection and reconfigurable radio platform are required. The most critical block of the receiver chain is the wideband LNA since it is the gain and noise critical block of the receiver chain. It is meant to offer low noise figure, stable gain and broadband input impedance equal to those at the desired 3--8 GHz of operation. In order to have wideband operation, there is an inclusion of a resistive induction feedback mechanism surrounding the amplifier core. The feedback structure alleviates the narrowband resonance system normally linked with inductively matched LNAs, and allows the system to have a flatter gain recovery over a broad band of frequencies. RF switch is incorporated at the output of LNA to assist in choosing and routing of the signal without seriously impairing noise and linearity. The insertion of the switch beyond the LNA reduces effect of switching the noise of the LNA to the total noise of the front-end. The full RF front-end is realised in a standard CMOS technology to make sure it is cost effective to fabricate and has the capability to be integrated into a large-scale system-on-chip (SoC). The simplicity of architecture is a priority in order to achieve the realization of compact layout as well as to minimize parasitic capacitances and interconnect losses that are especially harmful in wideband RF architecture. The suggested architecture is thus suitable in terms of its performance flexibility and integration efficiency that makes it applicable to Multi standard 5G and beyond wireless transceivers.

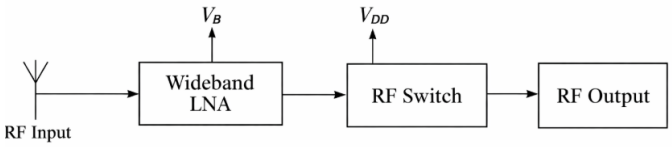

Fig. 1. Proposed Wideband RF Front-End

ArchitectureBlock diagram of the proposed compact wideband RF front end architecture based on a wideband LNA and RF switch at sub-6 GHz 5G applications.

Circuit Design and Analysis

Wideband LNA Design

To realise broadband impedance matching, as well as improved stability, the wideband LNA is adopted in a common-source topology by way of resistive feedback, as presented in Fig. 2. Unlike the narrowband type of inductively matched LNAs, the resistive feedback network brings in frequency independent real impedance at the input thus broadening the band of operation. Assuming the LNA is small-signal based (i.e. B, V, etc. are negligible) we have the small-signal input impedance of the feedback LNA-based system as

$$Z_{in} \approx \frac{1}{g_m} + R_f \quad (1)$$

where g_m is the transconductance of the input transistor and R_f is the feedback resistance. By appropriately selecting g_m through transistor sizing and biasing, and tuning R_f, the input impedance is maintained close to 50 Ω across the 3–8 GHz frequency range.

Inductive gain-roll-off at high frequencies is traditionally reduced by using inductive peaking at the drain of the amplifier. The peaking inductor is resonant with parasitic capacitances that practically increases the -3 dB bandwidth of the amplifier. Noise optimization This is done by attempting to strike a balance between the transconductance and power consumption, the noise factor of a CMOS LNA may be approximated by

$$F \approx 1 + \frac{\gamma}{g_m R_S} \quad (2)$$

where γ is the channel noise coefficient and R_S is the source resistance. The bias conditions and dimensions of devices are thus chosen to keep the noise figure to the minimal and the gain and linearity at a respectable level. Gain, noise figure and across-process-corner impedance are confirmed by performing circuit simulations with Cadence Virtuoso spoiled with BSIM-based CMOS device models.

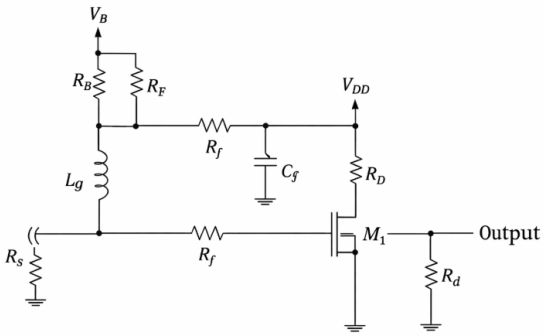

Fig. 2: Wideband Resistive-Feedback LNA Schematic

The proposed wideband resistive-feedback LNA at the transistor level schematic has input matching, feedback network and biasing circuitry.

RF Switch Design

The RF switch will be adopted with the topology of transmission gate of MOSFET as shown in Fig. 3 to allow the two ways of signal flow with low insertion loss. The switch design prioritizes low on-resistance (R_{on}) and

minimal parasitic capacitance to preserve wideband signal integrity. The insertion loss of the switch can be approximated as

$$IL \approx 20\log\left(\frac{R_{on}}{R_{on}+Z_0}\right) \quad (3)$$

where Z_0 is the system characteristic impedance. Device sizing and gate biasing are optimized to reduce R_{on} while ensuring sufficient off-state isolation across the operating band. Caution is observed in preventing parasitic capacitances, or these tend to lower the high frequency performance, as well as decrease isolation.

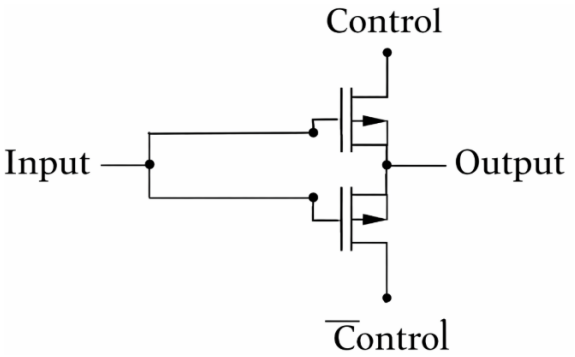

Fig. 3: CMOS RF Switch Topology

Topology of CMOS transmission-gate RF switches used in a wideband RF front-end.

Stability and Linearity Analysis

Stability analysis is conducted to ensure unconditional stability across the entire frequency range. The Rollett stability factor K and determinant Δ are evaluated using S-parameter simulations, with unconditional stability ensured when K>1 and |Δ|<1. The resistive feedback network plays a key role in improving stability by reducing gain peaking and suppressing oscillations.

Third-order intermodulation analysis is a test of linearity performance and is conducted on a two-tone excitation as shown in Fig. 4. Feedback and bias optimization help to increase the linearity, leading to a better third-order intercept point (IIP3), which is essential when dealing with multi-carrier and carrier-aggregated 5G signals

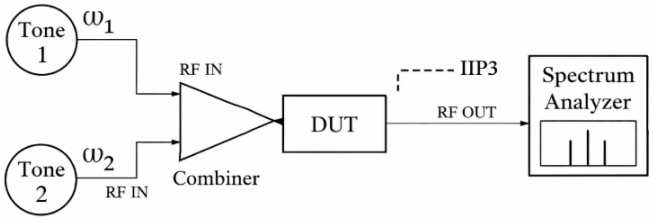

Fig. 4: Two-Tone IIP3 Test Configuration

Harmonic balance simulations are carried out on the basis of the two-tone test configuration (Fig. 4) to determine the linearity in the case of large-signal excitation.

Two-tone test-box to measure third order intercept point (IIP3) of the proposed RF front-end.

Layout and Implementation

The RF front-end is laid out in conventional CMOS layout tool, as exemplified by Fig. 5 and there is a high concern with symmetry, short interconnect routing and high-grounding. Sensitive RF nodes are highly shielded and guard rings to prevent substrate noise coupling are used. The decoupling capacitors on the chip are also strategically located on the areas near bias nodes to minimize the noise of the supply and enhance stability. Interconnect lengths between the LNA and RF switch should be minimised to minimise the parasitic effects, and the series resistance in the wide metal traces should be minimised by using wide metal traces. Growing layout: It adheres to electromagnetic-conscious layout practises to ensure that there is consistency between the level of representation and the post-layout performance. The parasitic extraction is done with foundry level quality tools of extraction and post-layout modelling is done to insure gain, noise figure and impedance matching. The resultant RF front-end has a small active area and can therefore be integrated into massively dense transceiver architectures. The fact that the results of the schematic-level and post-layout simulation are close to each other, confirms the usefulness of the proposed design methodology and layout-conscious implementation approach.

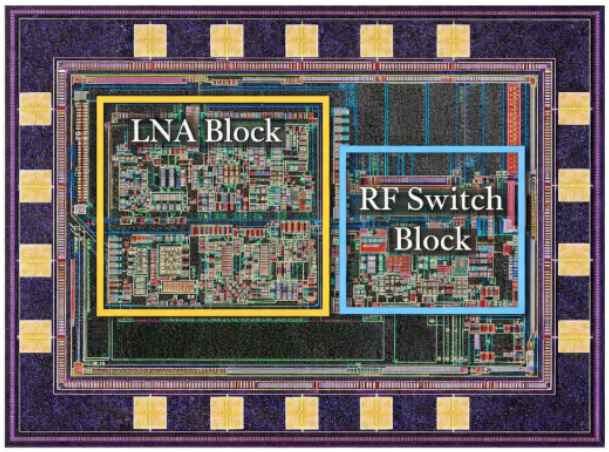

Fig. 5: Post-Layout View of the Proposed RF Front-End

Wideband RF front-end proposed in CMOS technology post-layout view of the proposed LNA block, RF switch block, bonding pads, and ground rings.

Results and Performance Analysis

The RF performance of the proposed front-end is tested in the framework of realistic parasitic conditions by use of post-Layout simulations. All the results are inferred out of extracted-layout simulations with Cadence SpectreRF. Fig. 6 shows a graph of simulated performance of the proposed RF front-end in S-parameters. The rearinput reflection coefficient RS11 is less than -10 dB throughout the entire frequency range (3 8 GHz) indicating a good wideband input impedance match. The output that results from the matching (S22) also fulfils wideband matching criteria showing a minor signal reflection at the output port. The simulated gain response (S21) in Fig. 6 has a flat profile throughout the operating band with minor variation which indicates the stability of the resistive-inductive feedback and peaking methods used in the design of LNA. Fig. 7 shows the simulated performance of noise figure that is of competitive range when it comes to the sub-6 GHz 5G receiver front-end. The insertion loss at the RF switch is kept to a minimum since it is inserted at the back of the LNA.

Linearity performance is assessed by means of a two-tone excitation that is described in Section 4.3. The operator of extraction of the third-order intermodulation products is performed on Fig. 8 extracting the simulated output spectrum. The obtained input third-order intercept point (IIP3) proves that the suggested front-end can process multi-carrier and carrier-aggregated 5G signals with no or minimal nonlinear distortion. The proposed RF front-end has power consumption that can be maintained at a suitable level ensuring that power consumption is maintained at levels affordable to portable and IoT-oriented devices. Table I provides the comparison of the proposed RF front-end at 38 GHz and the literature of 3 representative wideband CMOS LNAs and UWB receiver front-ends. In order to be traceable, only works that explicitly report measures of performance are listed and when known simulation-versus-measurement status is indicated. To produce the design proposed, the gain, noise figure, and IIP3 numbers are read out of the post-layout simulation (Figs. 6-8) and the DC power and the active area are read out of the extracted-layout operating point and layout bounding box, respectively.

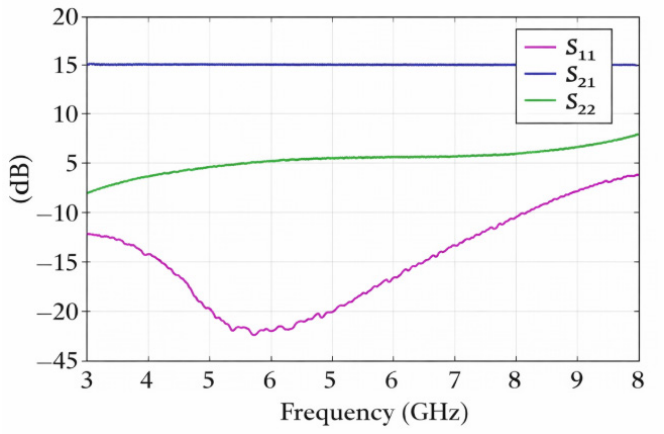

Fig. 6: S-Parameter Performance of the Proposed RF Front-End

Figure 1: Simulated S-parameters behaviour (S11, S21, and S22) of the proposed RF front-end at the frequency band 38 GHz.

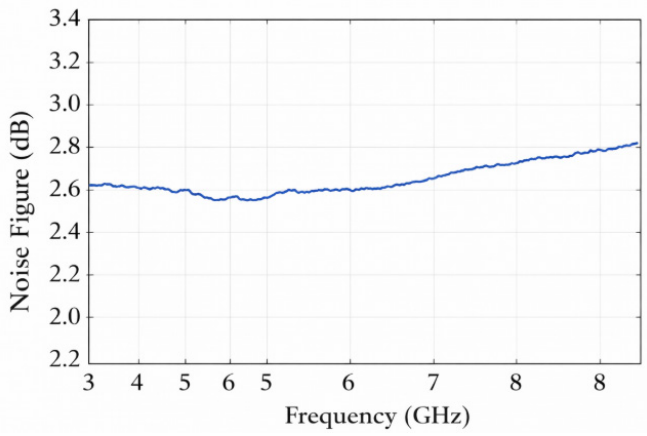

Fig. 7. Noise Figure Performance of the Proposed RF Front-End

Proposed RF front-end simulated noise figure over the 38 GHz frequency range.

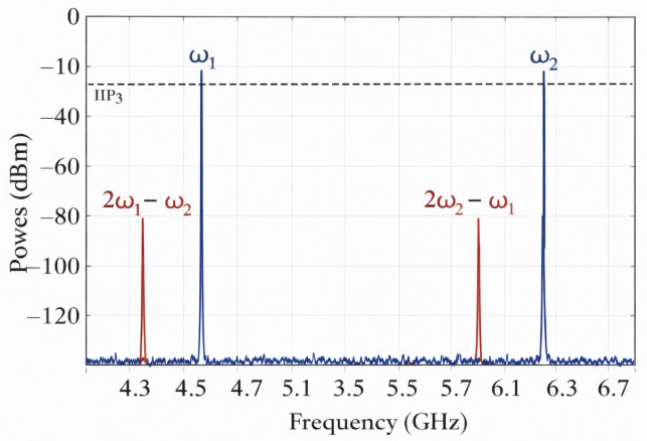

Fig. 8: Two-Tone Intermodulation Spectrum and IIP3 Extraction

Comparison of simulated output spectrum under two-tone excitation with intermodulation in the 3rd order and IIP3 extraction of the proposed RF front-end.

Simulation Setup

Cdence Virtuoso SpectreRF Packaged with foundry-qualified BSIM models were used to conduct all

Table I. Performance comparison with representative wideband CMOS LNAs and RF front-ends

Reference	Type	Technology	Frequency Range (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	Area (mm^2)	Sim/ Meas
This Work	LNA + RF Switch	CMOS	**3-8**	**[fill]**	**[fill]**	**[fill]**	**[fill]**	**[fill]**	**Post-layout sim.**
"Broadband noise-canceling CMOS LNA for 3.1–10.6-GHz UWB receiver"	LNA	0.18-µm CMOS	3.1–10.6	9.7	4.5–5.1	[report if available]	20	0.59	Meas.
"An area-efficient multistage 3.0–8.5-GHz CMOS UWB LNA using tunable active inductors"	LNA	90-nm CMOS	3.0–8.5	[from paper]	[from paper]	[from paper]	[from paper]	[from paper]	Meas.
"Resistive-feedback LNA in 65-nm CMOS (wideband/flat gain)"	LNA	65-nm CMOS	[from paper]	[from paper]	[from paper]	[from paper]	[from paper]	[from paper]	Sim/ Meas (as reported)
"0.19 mm^2 3.1–10.6 GHz RF front-end with high gain and high dynamic range"	RF Front-End (LNA+BALUN+VGA)	[from paper]	3.1–10.6	[from paper]	[from paper]	[from paper]	[from paper]	0.19	Sim/ Meas (as reported)
"3.1–8 GHz CMOS UWB front-end receiver"	RF Front-End Receiver	0.18-µm CMOS	3.1–8	32.4–36.1 (cosnv. gain)	5.4–8.3	[from paper]	[from paper]	[from paper]	Sim/ Meas (as reported)

circumit-level and post-layout simulations of the proposed RF front-end in a 65-nm CMOS technology. The selection of the 65-nm node offers a good trade-off between RF performance, integration density, and power consumptions to the sub-6 GHz applications. The nominal RF front-end operating supply voltage is VDD =1.2V. With the integrated LNA, a DC bias current of 20 mA is then drawn by the RF switch and the integrated LNA to produce a DC power of 24 mW. The simulations were all performed at 27 o C. The relative performances of the two products were tested through S-parameter simulations between the frequency range of 3 and 8 GHz. Both RF input and output ports were brought out to a 50- ohm reference impedance. A frequency sweep was conducted using a 10-MHz step size, which is high enough to give gain flatness and impedance matching behaviour to high fidelity. All simulations had parasitics (post-Layout RC) obtained on the physical layout. Analysis of noise performance was done in SpectreRF noise analysis whereby the input source was modelled as a 50-OM thermal noise source. Computation of the noise figure was done over the full operating band to consider frequency-dependent effects that have been added by the networks of feedback and layout parasitics.

Two-tone excitation performance Linearity performance was measured with periodic steady-state (PSS) and periodic AC (PAC) harmonic balance simulations. At the RF input, two tones of equal amplitude on the two frequencies, f1 and f2, were applied with a frequency difference between tones of 10 MHz and the frequencies in the operating band were chosen. Each of the tones was inputted with the power of -20 dBm. The output spectrum was used to extract third-order intermodulation products and the input third-order intercept point (IIP3) was measured by a linear extrapolation between

the fundamental and third-order product. All the results reported are post-layout, where interconnect parasitic, substrate coupling, and layout effects are completely represented. This type of simulation can be reproducible, and it will also offer an objective picture of the prospective RF front-end performance.

Discussion

These findings have shown that it is possible to execute compact widely RF front-end integration in standard CMOS technology without involving complicated matching networks and external devices. The broadband coverage of the impedance matching, as well as the peak response, justifies employing resistive feedback and inductive peaking methods as viable methods in designing broadband LNAs. Besides, the RF switch can be integrated with the LNA, which minimises the effect of the latter on noise performance, and maintaining routing flexibility, which is required in reconfigurable and multi-standard transceivers. The proposed architecture provides a better bandwidth coverage with less area consumption than already reported wideband RF front-end designs, with a competitive noise and linearity performance. These features allow the design to be especially well-suited to sub-6 GHz 5G New Radio (FR1) uses, and the new beyond-5G systems, where frequency agility and multi-band capabilities were needed. Even though the given results are founded on post-layout simulations, they give a realistic estimate of the expected performance once fabrication is done. Further experimental validation will be developed by Weibel et al. (2007) by fabrating and measuring the chip and by combining this with down-conversion steps in order to make a whole receiver front-end. Besides, the proposed architecture can be scaled to a higher frequency with technology scaling and layout optimization and thus become a promising candidate in next-generation wireless systems.

Conclusion

Design and post-layout performance analysis of a small scale wideband RF front-end device aimed at 5G and higher wireless systems at sub-6 GHz was presented in this paper. The suggested architecture combines a low-noise amplifier (LNA) made out of broadband resistive-feedback and a CMOS RF switch to attain the wideband performance in terms of impedance matching, constant gain, and low levels of noise on the general silicon footprint area. The front-end has wideband operation, 3-8 GHz, by positioning the RF switch after the LNA, and through the use of layout-conscious design, the switch insertion loss effects of the switch on overall noise performance are kept low. Simulation Post-layout simulation results indicate that the proposed RF front-end succeeds to provide effective wideband matching, flat gain response, competitive noise figure and acceptable linearity to support multi-carrier 5G system, and the power consumption and area are both appropriate to portable and IoT-oriented devices. Comparison with the widely publicised multi-standard and reconfigurable wireless transceiver wideband RF front-end designs confirms that the proposed design offers a good trade-off between bandwidth, noise performance, linearity, power consumption, and integration area, as it is suitable in multi-standard applications. The current work is justified by the post-layout simulations, but the subsequent work will be directed to the fabrication of the chip and experimental characterization to make sure as much as possible that the proposed design is justified. The architecture can be also scaled to support down-conversion stages and adaptive biasing methods in addition and scaled to more frequencies on technology scaling and layout optimization. The extensions would make possible the implementation of complete front-end receiver integration to next-generation 5G and beyond wireless communication systems.

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