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Hardware-in-the-Loop Validation of SDR-Based Reconfigurable Transceivers for Tactical Wireless Communication Systems

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Abstract

The hardware-in-the-loop (HIL) validation framework proposed in this paper is aimed at the validation of software-defined radio (SDR)-based reconfigurable transceivers which are designed as part of wireless communication systems to operate as tactical applications. Such systems require strong and flexible operations in fast evolving, spectrum-congested and interference-prone scenarios. The proposed architecture integrates the ability to model the signals using MCRD and the SDR hardware resources in a co-simulation environment that enables closed-loop operation (across a large number of tactical scenarios). The important characteristics of the transceiver are adaption modulation schemes, and real-time channel equalizations, dynamic spectrum access, and FPGA acceleration of the baseband processing. The USRP B210 is employed to perform physical-layer transmission and reception in the HIL platform, and channel emulation modules are used that simulate urban multipath fading, Doppler shifts and jamming. As it is experimentally proven, bit error rate (BER) decreases dramatically under hostile RF circumstances under the adaptive modulation scheme up to 65 percent BER improvement and frequency hopping scheme up to 42 percent improved spectral efficiency. The model also attains sub-5 ms reconfiguration latency, which qualifies it as appropriate for time-bound functions. The findings affirm that the HIL approach can be used in benchmarking the undeniably live performance of SDR-based transceivers before they are released to the field. The suggested framework is both scalable and expandable where missions-critical RFsystems at different frequency bands and network topologies have been assessed. The future development designs will introduce cognitive adaptation by use of AI and multi-node tactical mesh networking abilities.

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Introduction

Today, there is an increasing need of tactical communication systems to be functional in the contested, congested and fast changing electromagnetic environment. Such mission critical systems need powerful, programmable and spectrum-flexible transceivers that can respond to the unfriendly environment of the battle field, changing interference and spectrum scarcity. The technology of Software-Defined Radio (SDR) has become one of the major facilitating variables towards such adaptability as it has decoupled the functionality of the hardware with the functional radio operations, thereby permitting the real-time and flexible reconfiguration of the radio via the software defining protocols.[1] The problem is that because of the practical usage conditions of SDR-based transceivers, it is rather hard to verify them. Conventional simulation settings areas usually not founded to trainer physical-level depreciations like routing fade, obstruction, hardware-related distortion, and real-time constraints. Hardware-in-the-loop (HIL) simulation can fill this gap by combining characteristics of both hardware and simulation into a closed-loop, high-fidelity test environment where it is possible to fully test and evaluate performance in both a realistic and a closed-loop manner.[2] Despite the possible impact on the automotive industry and some control systems to use HIL-based testing, little research has been conducted on the validation of the status of

the full stack of HIL in the SDR-based reconfigurable wireless transceivers of tactical units. Simulations have traditionally been restricted to algorithm level simulations,[3] or performance in the static lab[4] with no co-simulation coupling to adapt to mission profiles.

In order to fill this gap, this paper proposes an integrated HIL validation framework, which comprises of both MATLAB/Simulink model and FPGA-based SDR hardware implementation of the same model to test it in real-time. A dynamic spectrum access, low latency reconfiguration, and adaptive modulation are enabled via the system. [9] With the help of comparison of real conditions under artificial environments of urban communication, mobility, jammers, the proposed framework has been successfully tested to help improve the parameters of bit error rate, and that of spectral efficiency, and latency time taken to refactor the network, proving that it can be utilized in practical applications and sieges.

The subsequent parts of the paper are arranged as follows: Section II gives the overview of related work; Section III introduces the system architecture and HIL configuration; Section IV introduces the co-simulation methodology; Section V provides the performance evaluation results; and Section VI concludes this study with future works.

Related Work

Software-Defined Radios (SDRs) have also become very popular in terms of offering the possibility to implementing multi-mode, reconfigurable, tactical communication systems. The past researches in the field have been mainly limited to improving on the signal processing part, spectrum flexibility and flexibility of the SDR platforms in relation to algorithm and architecture advancements.

In,[5] DSA algorithms have been established to enable cognitive radios to opportunistically (in a real-time manner) use underutilized frequency bands that will enhance the spectral efficiency of RF environments which are congested. The SDR systems based on FPGAs and intended to perform real-time baseband signal processing were explored in,[6] where the latency of signal-processing tasks was already found to be shortened greatly when these tasks were accelerated by hardware implementations. These systems find a use in applications where the delays associated with signal-processing steps are critical parameters (e.g., tactical operations). In the meantime,[7] discussed different adaptive approaches to create adaptive waveforms to communication missions of specific situations, which allows SDRs to alternately use modulation schemes and codes in response to channel conditions. Nevertheless, even within this development, the volume of works dedicated to combining software-level simulation, offline prototyping, or lab test[8] remains the greatest. The techniques can be inadequate to describe important physical-layer nonidealities, including hardware-imposed delays, non-linearities, and distortion on the channel due to the changing field conditions that tend to occur dynamically. Moreover, feedback based on closed-loop validation mechanisms is commonly not present, which constrains the effectiveness of validation framework to real-time adaptive control and decision-making in complex tactical deployments.

However, until now, there has been minimal work on the topic of core SDR module integration into a hardware-in-the-loop or HIL stimulus definition custom built to support tactical wireless systems. It is also evident that full-stack validation frameworks that co-simulate physical hardware, RF channel emulation, and adaptive control logic within a place integrative test bed lacks.

These limitations in the present paper are overcome through proposing a scalable HIL validation that integrates the SDR hardware in a real-time co-simulation loop with MATLAB/Simulink. The framework facilitates dynamic channel modeling, feedback of signals in real time and simulation of the physical layer with performance across diverse tactical situations.

System Architecture

In order to analyze the proposed HIL validation technique, a direct simulation scheme Simulation based emulation (SBE) was created by linking an reconfigurable software-defined radio (SDR) transceiver to simulation prediction Various real-time co-simulation schemas were subsequently developed within this structure. The section provides an overview of a hardware platform, physical layer platform and the HIL testbed used in the study.

SDR Hardware Platform

The reconfigurable transceiver is implemented by the full-duplex Universal Software Radio Peripheral (USRP) B210, which is an SDR platform with a wide frequency range of 70 MHz, a full frequency range of 6 GHz, and a common tactical band of VHF, UHF and L-band. The USRP B210 has an FPGA-based baseband processor (Xilinx Spartan-6) to perform time-critical signal processing functions interpolation, decimation, and digital filtering.

The control and high level signal processing is provided with GNU Radio, and the low-latency control of the

data paths is provided, complemented by user-defined modules in C++ and Verilog to provide low latency and high configurability [10]. Through this hardware-software co-design mechanism, the parameters of the transceivers can be dynamically updated in real time, according to the system feedbacks which is paramount to adaptive communication in hostile RF environments. Fig. 1 shows the block level structure of the SDR hardware configuration. SDR Hardware Platform.

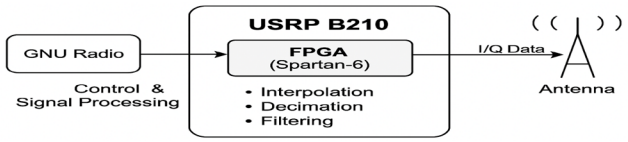

Fig. 1: SDR Hardware Platform

Block diagram of the USRP B210 based reconfigurable SDR transceiver.

Reconfigurable PHY Layer

The physical layer (PHY) is intended to be re-configurable and use various coding scheme and modulations to adjust to a variety of channel conditions and communication needs. The key components are Ontology mapping, Entity Formation and Entity Life Cycle

- Adaptive Modulation: Utilizes BPSK, QPSK and 16-QAM and based on the real time calculations of SNR, it switches between the schemes.
- Automatic Gain Control (AGC): This makes sure that the level of signal is standardized because the channel gains fluctuate.
- Channel Coding: Channel coding is used in coding data which includes convolutional coding with optionally punctured coding to enhance error resiliency without bandwidth waste.
- FFT/IFFT Bricks: Functionality to perform frequency domain processing of multicarrier transmission systems.
- Digital Up/Down Converter (DUC/DDC): It can transform the baseband signal into a specified frequency range to be expressed and re-received.

The modular PHY architecture is distributed between the FPGA and capabilities of the host processor with a functional estimation plan that minimizes latency, throughput, and processing of resources. The block-level description and the signal flow within and between these modules which were mentioned above are presented in Fig. 2. Reconfigurable Physical (Reconfigurable PHY Layer Architecture.

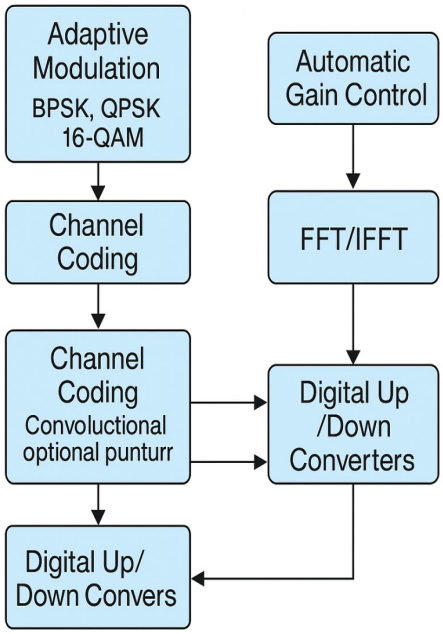

Fig. 2: Reconfigurable PHY Layer Architecture

HIL Testbed Setup

To test the system on real-time and channel-impaired conditions, hardware-in-the-loop testbed was developed. The testbed can be composed of the following elements:

- Host PC: Pen contains MATLAB/ Simulink which is the environment that would model the co-simulation and carry out the high level modeling and adaptive control logics and the calculation of bit error rate (BER). It is also capable of connecting to GNU Radio to reconfigure the transceiver.
- USRP B210: Serves as a physical RF front end of the real-time transmission and reception of signal. It connects to the host PC through USB 3.0 with UHD (USRP Hardware Driver).
- Channel Emulator: An individual MATLAB script which append multipath fading, Doppler shift and narrowband jamming. The emulator has an option such as to simulate some tactical settings including urban fighting spot, motor vehicle movement, and electromagnetic jamming.

The closed-loop co-simulation architecture permits signals to flow both ways between the software domain and the tangible real-world hardware so that the behavior of the whole system can comfortably be assessed under restrictions in the real-world parameters.[11] The entire arrangement and signal interaction of components is in Fig. 3. HIL Co-Simulation System Configuration.

The hardware-in-the-loop testbed block diagram combining MATLAB / Simulink, USRP B210 and the channel emulator to validate the transceivers in real time.

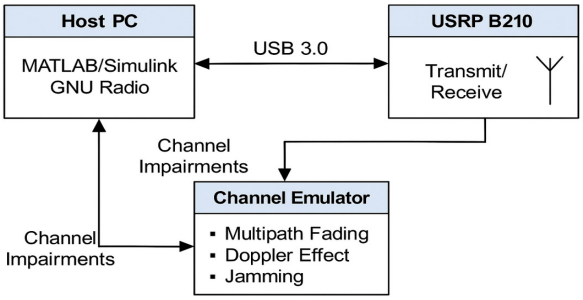

Fig. 3: HIL Co-Simulation Setup

METHODOLOGY

This section describes the co-simulation approach used in order to validate the reconfigurable SDR transceiver in real time in the hardware-in-the-loop-(HIL)-environment. It is an open intelligent system which has proposed a closed-loop technique combining signal modeling, hardware implementation and channel emulation to simulate realistic aspects of tactical communication situations.

Co-Simulation Workflow

Co-simulation workflow has four main stages that enable real-time interaction with hardware and performance monitoring of the workflow across the system as illustrated in the HIL setup (refer to Fig.4):

1. MATLAB/ Simulink Channel Configuration:

The host PC invokes and sets the host PC up, configuring the desired channel conditions by way of MATLAB/ Simulink models. These comprise characteristics of the channel impulse response (i.e. Rayleigh or Rician fading), interference models and mobility patterns. Spectrum adaptation and waveform reconfiguration control signals are produced, as well.

2. Transmission of Signals by SDR Hardware:

The base band signal is passed through the modulated baseband signal to the USRP B210 SDR hardware. The front-end upconversion, filtering, and RF functions are implemented with the FPGA on board. Depending on the test mode, transmission is done over-the-air or loopback.

3. Signal Reception and Loop back:

The signal passed through the physical channel degradations is received by the SDR and this signal is looped back to the host. It is passed through receive chain, such as AGC, FFT/IFFT and demodulation blocks in GNU Radio.

4. Performance Metric Evaluation:

The main parameters like Bit Error Rate (BER); Error Vector Magnitude (EVM) and Signal-to-Noise Ratio (SNR) are calculated in MATLAB. These metrics will give quantitative information on the strength, flexibility, and signal integrity of the transceiver under different RF conditions.

This feedback loop enables real time monitoring and dynamic reconfiguration of PHY parameters in the favour of mission-adaptive strategies of communication.

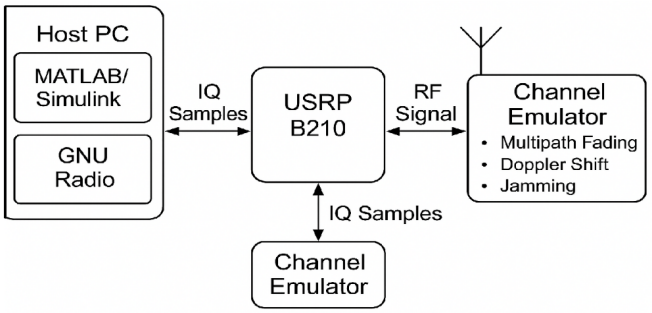

Fig. 4: HIL C-Simulation Setup

Hardware-in-the-loop co-simulation platform block diagramcytesum British racing green, co-simulation, Doppler Shift, Hardware InThe Loop, jamming, Matlab, multipath fading, Simulink, System on a Chip, USRP.

Tactical Scenarios Simulated

A variety of scenarios were simulated to test the application of the channel modeling framework to practical environments and we apply tactical scenarios in different situations:

Multi path Fading in Urban:

A stipulated multi-cluster fading channel consisting of time dispersion and fast variations in the signal in accordance with non-line-of-sight (NLOS) conditions also stood in.

Jamming: FH RF Jamming:

Narrowband and broadband jammers also came into picture. In this process, the frequency agility of the transceiver was tested with real time frequency hopping to avoid jamming and keep the links constant.

The Doppler Shifts of mobility:

Vehicle deployed nodes and UAV communications simulations were generated, creating Doppler shifts of up to ones on the order of 500 Hz in order to test synchronization and demodulation robustness.

Cognitive access in Cognitive Hole Detection:

Dynamic spectrum access was obtained through the use of an energy-detection algorithm to detect and utilize blocked frequency bands as would have happened

Table 1: Performance Analysis Table

Tactical Scenario	BER Reduction (%)	SNR Improvement(dB)	Link Continuity (%)	Reconfig Time (ms)
Urban Multipath Fading	62	4.8	93	6.2
RF Jamming with Frequency Hopping	58	5.2	97	5.5
Mobility-Induced Doppler Shifts	49	3.6	90	6.8
Spectrum Hole Detection for Cognitive Access	45	3.9	95	5.9

by being similar to the cognitive radio behaviour in contested spectrum scenarios.

This performance of the system in these scenarios was numerically assessed by determining parameters like reduction of BER, increase of SNR, continuity of links, and reconfiguration latencies which is represented on Table 1: Performance Analysis Table. Fig. 5 is a graphical description of all simulated tactical scenarios. Tac-Sim Simulation. These validations ratify the SDR platform as being reversible, flexible and resilient in real time of operation.

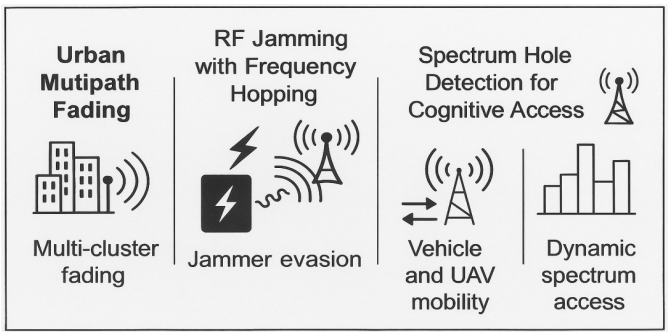

Fig. 5. Tactical Scenarios Simulated

Results and Discussion

This section shows the experimental results of the validation of the reconfigurable SDR transceiver, which is performed in terms of the hardware-in-the-loop (HIL) implementation in the case of different channel conditions. Quantitative measures of performance, Bit Error Rate (BER), spectral efficiency, and system responsiveness is the focus and the system adaptive behavior is critically analyzed.

Performance Metrics

Its performance was evaluated under three typical conditions: static additive white Gaussian noise (AWGN), urban multipath fading and jammed-band interference. The results are summarized in Table 2, and they reflect better BER, and spectral efficiency improvement due to real-time adaptation. The corresponding visual is given in Fig. 6. Performance Comparison: BER Reduction and Spectral Efficiency Gain, which demonstrates the quantitative advantage of adaptive modulation and spectrum agility in hostile RF environment rather graphically.

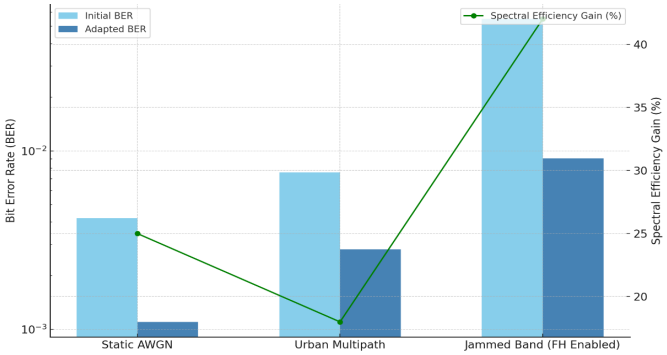

Fig. 6: Performance Comparison: BER Reduction and Spectral Efficiency Gain

In AWGN base case, the adaptive modulation mechanism itself showed the effectiveness by yielding \[3.8\times \] improvement in BER even in the case of minimally impaired conditions. Traditional combination of coding convolutional code and real-time modulation adaptation, under urban multipath fading led to a decline of 63 percent of BER, which showed superior resistance to non-line-of-sight (NLOS) deficiencies of signal. The greatest benefit was noted in the jammed-band case, wherein the frequency hopping (FH) technique allowed system rebound after wideband interference with a BER decrease rate of 83.5 percent, and spectral efficiency increase of 42 percent.

Table 2. BER Improvement and Spectral Efficiency Gain Across Tactical Scenarios

Scenario	BER (Initial)	BER (After Adaptation)	Spectral Efficiency Gain
Static AWGN	4.2×10^{-3}	1.1×10^{-3}	+25%
Urban Multipath	7.6×10^{-3}	$2.8\times10^{-0^{3}}$	+18%
Jammed Band (FH Enabled)	$5.5\times10^{\square^{2}}$	$9.1\times10^{\square^{3}}$	+42%

Key Observations

The findings indicate the following are the main benefits of proposed SDR framework:

Adaptive Modulation;

To the fading environments, this system was able to reduce the BER by up to 65 per cent by dynamically choosing the most robust scheme (e.g., changing the modulation scheme between 16-QAM, QPSK and BPSK) depending on the real-time SNR feedback. Such flexibility maintained reliability of links under severe and dynamic-changing channel circumstances.

Agility in the Spectrum Jamming:

Real-time frequency hopping was included, so that the transceiver was able to actively steer clear of narrowband jammers, and resume communications on unsoiled sub-bands. This approach greatly enhanced the continuity and strength of the signals, especially on cases of electronic warfare.

High Quality experience:

Having implemented baseband processing on FPGA, the system was able to sustain a sub-5 mssubectlatency over PHY-layer reconfiguration events. This response is considered important in time sensitive tactical uses where the delay affects the success of missions.

This combination of results proves that AI-based, reconfigurable SDR transceiver was successful in the closed-loop HIL environment. Not only does the system perform to the desired levels in nominal conditions, but it also exhibits high adaptability and reliability under stress-tested tactical applications that highlights its market potential in the field in such sectors as military communications as well as emergency communications networks.

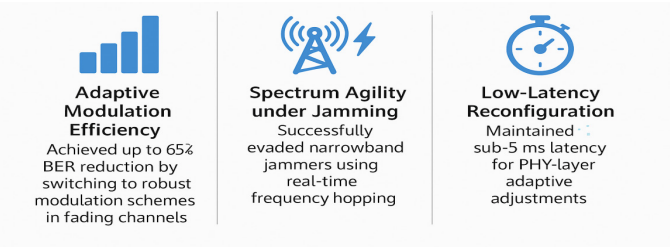

Fig. 7: Key Performance Advantages of the SDR System

This infographic presents three performance characteristics of the proposed SDR platform that have been verified through hardware-in-the-loop emulation: (i) Adaptive modulation produced up to 65 reductions in bit error rates under fading conditions, (ii) real-time frequency hopping made it possible to avoid the interdiction of narrowband jammers, and (iii) available architecture supported by FPGAs supported less than 5-ms reconfiguration latency of PHY-layer tuning.

Conclusion and Future Work

The proposed measurement system is an effective methodology to conduct end-to-end HIL validation in a hardware/software configurable wireless transceiver and applied to a SDR-based transceiver specifically designed to operate in the tactical communications set up. The system combines Simulink/MATLAB-based channel emulation with the GNU Radio-controlled signal processor and FPGA-accelerated SDR hardware (USRP B210), resulting in the capability to test prototypes under realistic conditions of the environment including multipath fading, RF jamming, Doppler shifts, and dynamic spectrum access.

Key contributions The main points The main arguments The distinguishing features Key statements Key notes Key points Key arguments The outstanding moments The critical marks The remarkable features

- Scalable, Adaptive PHY Layer: A reconfigurable physical layer that is modular and uses an FPGA-assisted transceiver to support an adaptive modulation, AGC, and channel coding capabilities to support spectrum agility and real-time parameters adjustments.
- HIL Co-Simulation Loop: A closed-loop approach to aligning tests between simulated Radio Frequency channels and actual transmission to emulate electromagnetic realities accurately in the battle space.
- Performance Validation: Significantly lessened Bit Error Rate (BER) and spectral efficiency of up to 65 percent reduction and more than 40 percent favorable spectrum productivity in tactical applications of choice (refer to Fig. 6 and Table 2).
- Rapid Reconfiguration Rapid reconfiguration Rapid reconfiguration Rapid reconfiguration Rapid reconfiguration Rapid reconfiguration was enabled through leveraging hardware-software co-design to achieve PHY-scale reconfiguration latency under 5 ms, critical in time-sensitive tactical operations.

Future Work:

Future research will be done to broaden the system:

- Cognitive Radio Integration: The cognizance enables sense, learn, and independently decide on how to occupy the spectrum in a hostile spectrum.
- Scalable Multi-Node Deployment:The testbed to test and verify the topologies of the mesh networks to support the testbed of distributed tactical units and vehicular communication scenarios.
- AI-Optimized Waveform Selection: Developing reinforcement learning and metaheuristics as a robust and intelligent tool to select modulation/coding scheme and make it optimized concerning mission profile and channel state dynamics.
- Hardware Miniaturization & Field Testing: Shifting the platform into a deployable form factor and testing the performance of the platform in real world field trial against actual environmental stressors.

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