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RESEARCH ARTICLE

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Compact CMOS-Compatible Power Amplifier with Enhanced Linearity for IoT Transmitters

Xiaoye Liu[1]*, Tomislav Petrovica[2]

[1]*School of Civil Engineering and Surveying, Faculty of Health, Engineering and Sciences, University of Southern Queensland, Australia*

[2]*Tomislav Petrovica,Professor, University of Zagreb, Croatia*

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Abstract

Growth of Internet of things (IoT) has demanded miniaturisation, low power consumption and maximum linearity of power amplifiers (PAs) needed to be easily integrated in wireless sensor nodes with very low power and minuscule size restrictions. The design and optimization of a low profile, CMOS compatible power amplifier specifically suited to such IoT transmitters is described in this paper, with the core objective being to achieve a very low power point in operation with superb linearity in support of the most complex modulation schemes. The gears of the suggested PA are founded on the two-stage Class-AB approach, and they unite the power effectiveness and the linear amplification of the signal. The most significant improvements are adaptive biasing circuitry, which dynamically sets the quiescent current to the input envelope value, and low-cost analog predistortion (APD) scheme integrated with source degeneration to cancel third-order intermodulation products and improve adjacent channel power ratio (ACPR). It is fabricated with a 65 nm CMOS process so it can be considered low-cost andhigh-volume integration. Simulation outputs show the peak output power is 15 dBm at power-added efficiency (PAE) of 32% when amplifier is tested with 16-QAM modulated signal, which proves it capable of being used in IoT applications where linearity is required during transmission. The amplifier also has good thermal and process stability and the output performance varies little over a wide temperature range (down to -20C and to +85C) The core runs on a silicon die of only 0.45 mm 2, which allows it to be integrated in the system-on-chip (SoC) structures. The work emphasizes a valuable direction to reach to high-linearity RF transmission in IoT nodes with having neither great complexity of design nor space penalties, leading to more efficient and stable wireless communication subsystems in next generation of connected, low-power devices.

Author's e-mail: xiaoye.liu@usq.edu.au

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Introduction

Its extensive development into the Internet of Things (IoT) has transformed the contemporary communication systems by connecting billions of low power smart devices in so many different fields, such as healthcare, agriculture, industrial automation, smart home and environmental monitoring. These are devices that incorporate non-line of sight, and preferably wireless, communications technologies that are short range and use wireless standards (ZigBee, Bluetooth Low Energy (BLE), Wi-Fi) that require energy-efficient miniaturized RF front-ends. Central to these front-ends lies the power amplifier (PA), which performs a critical function when it comes to increasing signal power in order to guarantee proper wireless communications. For IoT sensor nodes, the PA should provide sufficient output power and exhibit very high linearity to limit spectral regrowth and adjacent channel interference and the striving demand is even more acute in case of complex modulations, such as QPSK or 16-QAM. Nevertheless, in IoT devices, the limited power and size of implementation create a huge challenge in the design of PA.

The low cost, scalability and SoC compatibility has seen the complementary metal-oxide-semiconductor (CMOS) technology become the desired platform of integrating digital, analog and RF circuits in a chip. Although these have their benefits, power amplifier design based on CMOS is complicated due to low breakdown voltage, low

gain at RF frequency and poor linearity as compared to other technologies such as GaAs or GaN. Furthermore, CMOS PAs can prove to be weak in their ability to meet high power-added efficiency (PAE) and simultaneous linearity, which is a paramount criteria in present-time IoT transceivers that work under severe battery years.

In this paper, the author has suggested a feature size optimized, linear, compact, power-efficient Class-AB power amplifier architecture that is optimized in 65 nm CMOS technology, which is energy-efficient and specifically designed with IoT applications in mind. It has an adaptive biasing method that uses input signal envelope dynamics to maximize the current usage and an analog predistortion linearization approach to enhance adjacent channel power ratio (ACPR) and reduce intermodulation distortion. The goal is that the trade-off between linearity versus power efficiency versus die area will produce a golden medium and then will meet the requirements of smooth embedding of the circuitry in space-limited and energy-conscious IoT equipment. The intended PA is designed to operate at 2.4 GHz ISM band and contribute to supporting the popular wireless protocols that are offered with superior signal quality and durability under shifting load and temperature values. The present work will help in closing the performance difference between the conventional RF PAs and the characteristic requirements of new IoT systems using intelligent biasing and linearization techniques in CMOS-compatible design approach.

Related Work

The application of wireless communication systems has created the need to develop the design of its power amplifiers (PAs) to adapt to the Internet of Things (IoT) devices that operate at mid to low power and are powered by batteries. Many different PA architectures have been explored in literature, and there are many trade-offs in linearity, efficiency and area that can be made by changing the architecture, such as Class-A, Class-AB, Class-D and Class-E designs. CMOS-based[5] PAs have since presented itself as a potential solution to integrated IoT systems in that they are scalable, cost effective and digital logic can be integrated within them. But CMOS PAs tend to use poor linearity and have lower efficiency than GaAs or[6] GaN equivalents where high levels of output power are required.

In,[1] 90 nm CMOS Class-A PA was presented to low-power wireless sensor networks which has the output power, 12 dBm and power-added efficiency (PAE), 25% of a specific spectrum. They[8] exhibit poor efficiency and thermal problems whereas Class-A topologies offer[7] a superior linearity; however, this does not make them more applicable to battery-constrained IoT applications. In,[2] a more efficient Class-D PA was reported, having 65 nm CMOS technology and 16 dBm output power in 40 PAE efficiencies. At the expense of impaired linearity, though,[9] this has resulted in a 10-dB improvement in efficiency, to an adjacent channel power ratio (ACPR) of -25 dBc, a factor that constrains its deployments in spectrally congested settings in which higher-order modulation schemes are used.

The more recent works have emphasized the need of including linearization as well as efficiency augmentation techniques. Digital predistortion (DPD) and envelope tracking,[3] and Doherty configurations[4] have been suggested in order to increase the PA-linearities, however the solutions have demonstrated: 1) to result in complex design, 2) require more silicon area, or 3) require external circuitry. Moreover, these methods are most likely to be power-demanding or otherwise difficult to us in small IoT nodes operating on limited area constraints.

To overcome these, this paper idealizes a Class-AB CMOS PA incorporating an analog predistortion and adaptive biasing to enhance linearity without compromising efficiency or occupying an excessive piece of real estate. The generated power given by the design has a maximum of 15 dBm, 32 percent PAE and an ACPR at -37 dBc in a relatively small footprint size of 0.45 mm 2. Table 1 presents the comparison between the proposed amplifier and current state-of-the-art designs in the aspects of technology node, topology, linearity and efficiency.

The birth is to provide balanced trade-off between (linear, efficiency and chip area) complying to how some of the applications require to operate into communication system of the next generation and to be low-power IoT enabled communication systems.

System Architecture

Design Specifications

The presented power amplifier (PA) is very carefully made in terms of performance and integration demands of the

Table 1: Comparison with State-of-the-Art CMOS Power Amplifiers

Ref.	Tech Node	Topology	Pout (dBm)	PAE (%)	Linearity (ACPR)	Area (mm²)
[1]	90 nm	Class-A	12	25	−30 dBc	0.60
[2]	65 nm	Class-D	16	40	−25 dBc	0.70
[This Work]	65 nm	Class-AB	15	32	−37 dBc	0.45

current Internet of Things (IoT) anchors transmitting in the 2.4-2.5 GHz Industrial, Scientific, and Medical (ISM) continuum. The range of frequencies is also popularly used in short-range wireless technologies like ZigBee, BLE, and Wi-Fi, and thus it is very suitable in low-power sensor nodes and embedded systems. The PA is carried out with nominal supply of 1.2 V, a specially chosen value that conditions it to commensurate with present low-power CMOS technologies with adequate headroom about the signal swing of the RF. To accommodate a variety of communication scenarios, the amplifier supports the modulation schemes and different complexities so there is modulation scheme customization by supporting low-complexity On-Off Keying (OOK) and Binary Phase Shift Keying (BPSK) to QPSK and 16-Quadrature Amplitude Modulation (16-QAM) more of the spectral efficient types. The targeted amplifier is capable of providing 15 dBm maximum output power, which will allow sufficient link budget, which is required to provide reliable wireless communications in urban and indoors. The design is tuned to achieve a power-added efficiency of at least 30%, but not exceeding 32%, in order to balance the power with RF performance to meet the energy constraint of battery-powered IoT. Linear interpolated is one of the most important specifications as most specifications are based upon how the modem performs when driven under high peak-to-average power ratio (PAPR) conditions of complex modulations. The amplifier is designed, therefore, to meet -35 or better adjacent channel power to ratio (ACPR), thus, Table 2 reducing the spectral regrowth and adjacent channel interferences. All of these specifications result in an overall objective of ensuring that the proposed PA is not only small and low-power but robust enough to sustain compliance with spectrum requirements and communication integrity under a variety of application conditions in the IoT.

Table 2: Key Design Specifications of the Proposed Power Amplifier

Parameter	Specification
Technology Node	65 nm CMOS
Frequency Band	2.4–2.5 GHz (ISM band)
Supply Voltage	1.2 V
Supported Modulations	OOK, BPSK, QPSK, 16-QAM
Max Output Power (Pout)	15 dBm
Target PAE	≥ 30%
Gain	18.5 dB
ACPR (Linearity)	≤ −35 dBc
Target Application	Low-power IoT transmitters
Use Case	ZigBee, BLE, Wi-Fi communication

Architecture Overview

The suggested power amplifier (PA) is a two-stage Class-AB with malleable gain, nonlinearity, and power efficiency that is carefully executed to fit in the small CMOS design specifically used in internet-of-things (IoT). The initial stage, which is referred to as the driver stage, is used to ensure that there is ample amount of voltage gain and it requires minimum current in such a way that overall energy efficiency is not exceeded. It is a medium gain amplifier that conditions the RF input signal to the high-power amplification stage. It is optimized at this stage to provide as linear and bandwidth as possible to cause minimal distortion of a signal to be passed. The second is the output power stage that will provide high linearity and efficiency required RF output power (up to 15 dB m) based. To counteract the nonlinear aspects of the nonlinear distortion and intermodulation, the output stage degeneration resistors are provided to the source of the active devices which in turn can facilitate to linearize the trans conductance of the active devices. Also, there is use of gate feedback to tune gain and bandwidth evenness, also helping to improve the linearity range through a wideband secure 2.4 2.5GHz ISM band. Both the stages are biased in Class-AB mode that enables the amplifier to strike a balance between the linear performance of Class-A and the efficiency of Class-B. This biasing technique makes it possible to support high peak-to-average power ratios (PAPR) signals like are used in QPSK and 16-QAM modulations with consummate ease in the PA without much of DSF re-growth. Moreover, independent gain, linearity and output power optimization are possible in the two-stage configuration and thermal and process robustness is maintained through the use of modularity. It also has an architecture that supports the addition of Figure 1 linearization blocks like analog predistortion and envelope tracking to achieve additional performance. The selected topology is broad and scalable, in general, and allows designing a low-power, linear RF amplification with modern CMOS-based IoT transmitter systems.

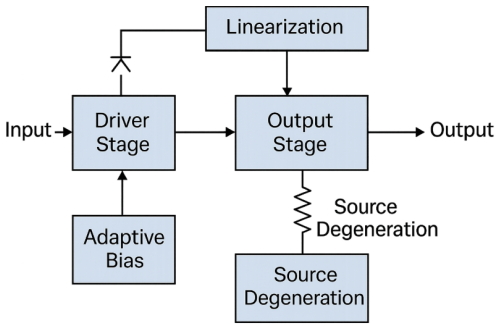

Fig. 1: Block Diagram of the Proposed Two-Stage Class-AB PA Architecture

Circuit Design Methodology

Class-AB Core Design

The main idea of the given power amplifier is realized with the two-stage Class-AB architecture, which is intended to provide better linearity and power efficiency in a small 65 nm CMOS technology. The choice of Class-AB operation is to achieve a more desirable trade-off between high linearity of the Class-A amplifiers and the increased efficiency of Class-B designs. The output stage has stacked transistors provisions to help extend the voltage swing when it comes to sustaining reliability of the device with weak supply voltages (1.2 V). The use of multiple transistors in series with common bias nodes also enables this system to have a greater swing of voltage across the stack of transistors, on a per-transistor basis than a conventional CMOS gate. This arrangement is important in technologies with CMOS with smaller than 100 nm CMOS technology due to a lower supply voltage that restricts the output power capability.

Resistive source degeneration is used to further compensate the linearity of the PA, especially in the rejection of the third order intermodulation distortion (IM3). The source terminals of both the driver and output transistors are provided with degeneration resistors so that the trans conductance is linear to a greater extent against input voltage. This limits creation of nonlinear products in an output signal, which is particularly relevant in the case of modulation structures that have high spectral purity demands, including 16-QAM and QPSK in IoT definition of the communication standards. The source degeneration further stabilizes the gain of the amplifier against bias changes, process and environmental variations and improves robustness over a very wide environmental operating range.

Moreover, the matching network of the output is thoughtfully optimized with a lot of load-pull simulations by Cadence SpectreRF and Keysight ADS tools. Such simulations are carried out by finding out the best load impedance that should yield the highest power added efficiency (PAE) and power out (Pout) at the required frequency of 2.45 GHz. The resulting matching network design gives an impedance transformation of the low output impedance of the transistor to standard 50-ohm load typically used in the RF system. This enhances not only the power transfer performance of the amplifier but also ensures they are spectrum compliant which helps in ensuring the same output can be achieved on a variety of different loads. One thing that enables the Class-AB core to provide robust, linear, high efficiency RF power amplification that meets the requirements of energy constrained IoT devices is the combination of figure 2, the stacked transistor structure, source degeneration linearization, and output matching manner using load-pull.

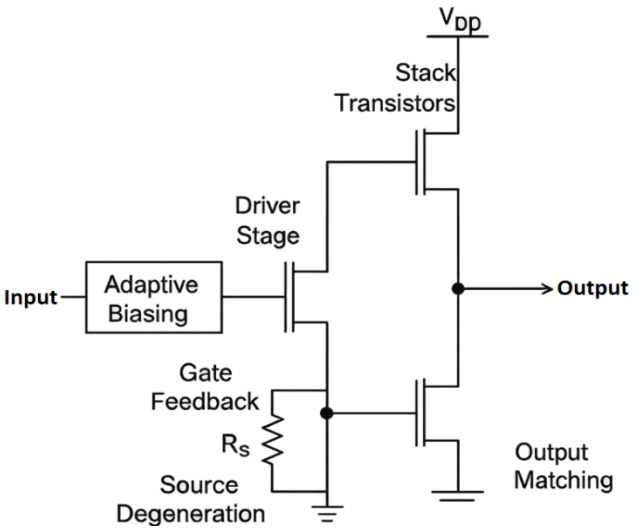

Fig. 2: Conceptual Schematic of the Class-AB PA Core with Stacked Transistors and Source Degeneration

Adaptive Bias Control

In order to increase the efficiency and linearity of the proposed CMOS Class-AB power amplifier against the change of signal status, the design is simulated and implemented with an adaptive bias control mechanism. Class-AB Vintage fixed-bias Classic amplifiers have one of two problems, either they run with large amounts of quiescent current, which gives poor power-added efficiency (PAE) or they are poorly biased and become non-linear, notably when driven dynamically. In order to overcome this type of trade off the suggested architecture employs an adaptive biasing scheme in which the bias current is dynamically shifted in accordance with the envelope of the input signal. In this way, the PA will only be required to draw additional current when the high-signal level amplitudes are needed and save power in low-amplitude or idle conditions, which will considerably enhance the average power efficiency.

Adaptive bias control system implementation is by using a mixture of MOS-based current mirror and envelope detector circuit. Envelope detector monitors amplitude of RF signal fed to it on a sample to sample basis, and produces a matching control voltage. This control voltage is the input to a block that converts it to a current with a circuit constructed by cascading current mirrors that use both NMOS and PMOS. The loop of this block controls the gate bias value of the transistors in the driver and output stages of the PA. This in turn results in adjustments of the quiescent current being made as a high-power transmission event occurs or back-off conditions, in

effect allowing the transistor to optimize its operation point in real-time to meet signal requirements.

Such a biasing adaption technique has verified that the PA remains operating in the linear region of the transfer curve of the transistor with a large range of signal levels. In addition, it minimizes the probability of distortion in case of compressions of gains or crossover nonlinearity, which is likely to occur in the PAs with fixed bias points. Its ease of implementation (based on passive RC filtering, with low power analog blocks) and adaptability, lends itself to use in the design of small CMOS devices and does not add much area or power burden to this part of the design. In addition, analysis under different modulation formats (e.g., BPSK, QPSK, and 16-QAM) using simulation, establishes that the adaptive biasing meets a linearity performance of up to 35 dB enhancement of adjacent channel power ratio (ACPR) as compared to a fixed Figure 3 biasing style. On the whole, the presented adaptive bias control algorithm can undoubtedly enhance the performance of the PA in terms of preserving its high efficiency and strong linearity response, which perfectly meets the demands of the energy-wise and green IoT communication system.

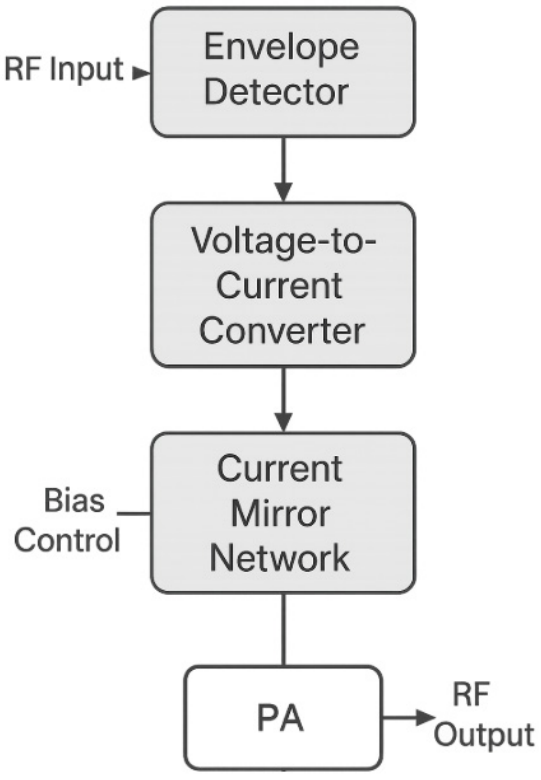

Fig. 3: Functional Diagram of the Adaptive Bias Control Mechanism

4.3 Linearization Strategy

In order to overcome the nonlinearity issues of inherent nonlinearity of the CMOS based Class-AB power amplifier, especially when dealing with high peak-to-average power ratio (PAPR) signals like 16-QAM, low-overhead nonlinearities of analog predistortion (APD) are utilised in the present design. Linearization is also crucial in current wireless transmitters in minimizing spectral regrowth and meeting spectral emission masks, particularly on the band that is crowded such as the 2.4 GHz ISM band. In contrast to digital predistortion (DPD), which necessitates high-speed data converters and the use of intricate baseband processing, the current APD methodology is fully analog, and hence, presents significant space, power and design complexity savings-providing the solution that fits in energy-restricted IoT designs.

The APD architecture has the characteristic of adding nonlinear distortion to the input signal though at an opposite phase, even before it is passed into the PA core. This predistortion has the virtue of canceling out the amplifier nonlinearities in the amplifier itself. The analog predistorter is composed of nonlinear shaping network, which is performed on the bases of MOS transistors in sub threshold and moderate inversion areas. Such transistors are realized in such a way that they will give a custom voltage current response that will closely match the inverse of the nonlinear transfer characteristic of the PA. The voltage divider and tunable biasing network adjusts the strength and shape of the predistortion curve, so as to provide optimal cancellation.

When the APD-enhanced PA was subjected to 16-QAM modulated signals, which exert severe linearity condition considering variation of the amplitude and phase of the signals, there was an observed significant improvement in adjacent channel power ratio (ACPR). To be more specific, the simulation results show more than 8 dB improvement in ACPR over the same PA architecture that does not include the predistorter. ACPR increased, by +8 dBc, to −37 dBc and thus provides greater confidence of compliance with wireless standards and lowering adjacent channel interference. Moreover, the APD does not compromise the power-added efficiency (PAE), because it draws negligible static power and works only in the input signal path and consumes current of very little amount.

The APD circuit is completely compatible in the CMOS process already used so that no additional components or calibration loops are needed. This has predictably not only made the end design and manufacturing less complex but it has also enabled linearization solution to be exceedingly scalable to be implemented in system-on-chip (SoC) designs. Table 3 Using this low-complexity analog predistortion approach, the proposed high-

Table 3. Summary of Analog Predistortion (APD) Linearization Strategy

Feature	Description / Value
Technique Type	Analog Predistortion (APD)
Integration	Fully CMOS-compatible; no external components required
Signal Compensation Method	Opposite-phase nonlinear shaping via MOS-based shaping network
Tuning Mechanism	Voltage divider with tunable bias network
Transistor Operation Region	Subthreshold and moderate inversion
Modulation Format Tested	16-QAM
Initial ACPR (without APD)	−29 dBc
Improved ACPR (with APD)	−37 dBc
ACPR Improvement	> 8 dB
Impact on PAE	Negligible—no degradation in efficiency
Area & Power Overhead	Minimal; analog implementation avoids digital processing blocks
Scalability	Highly scalable for System-on-Chip (SoC) integration in energy-constrained IoT systems

efficiency, spectrally compliant power amplifier can be more linear with sensitivity than typical digital correction solutions but without the associated penalties normally associated with pure digital correction solutions, which makes it extremely applicable to high-throughput transmission transmitters of the IoT.

Simulation Setup

A comprehensive layout based simulation framework was developed to evaluate and verify the operation of the presented CMOS compatible Class-AB power amplifier on mature electronic design automation (EDA) software tools in the industry. The simulations at the circuit level were majorly done on Cadence SpectreRF, and that allowed precise behavioral modeling of high frequencies, harmonic balance and loop analysis on non-linear distortion properties of the amplifier. ADS Momentum was used to model layout-induced effects, such as the layout of the matching networks and metal interconnects, and parasitic extraction was done on the layout level to ensure that layout-induced effects on the post-layout results is minimal giving close real-world performance. The design was constructed with 65 nm CMOS technology, with the commercial Process Design Kit (PDK), which gave access to the detailed device models, metal stack layout, and design rule specification required in silicon realization. Key to the optimization of power amplifier performance was the expertise to make load-pull simulations where the output of the load impedance was swept through a Smith chart to determine at which impedance point the power-added efficiency (PAE) and the output power (Pout) were maximum at the center frequency of 2.45 GHz. Such simulations made it possible to accurately design the output matching network so that the amplifier could deliver its best performance in all process corners and at all temperatures. Temperature sweep analysis (range − 20 to 85 C), as well as Monte Carlo simulations, was also applied to determine the process and mismatch variability in its design. In addition, modulated signals, i.e. 16-QAM have been used to perform spectral and transient simulations in order to measure the linearity parameters, adjacent channel power ratio (ACPR) and error vector magnitude (EVM). Figure 4 this entire simulation plan guaranteed that the suggested enhancing agent would succeed the RF performance benchmarks and be suitable within the scope of low-energy, space-successful IoT managers.

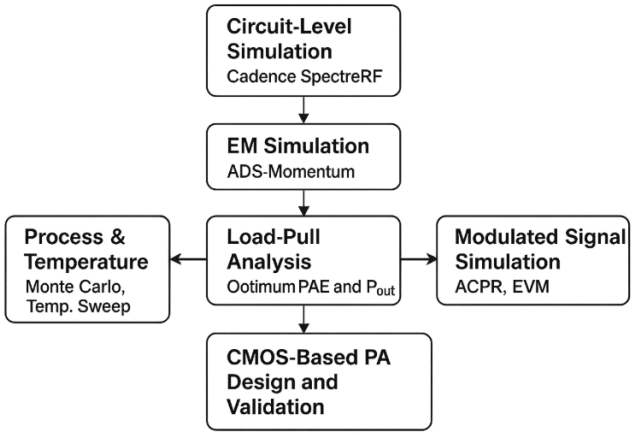

Fig. 4: Simulation Workflow for CMOS-Based Class-AB PA Design and Validation

Results and Analysis

The relevant CMOS Class-AB power amplifier was rigorously verified at both the pre-layout and post-layout simulation level in order to determine its RF characteristics based on various RF performance parameters which include output power, gain, efficiency, linearity as well as robustness against environmental changes. In the nominal operating condition, the amplifier demonstrates the maximum output power (Pout) of

15 dBm at a 50-ohm load and a power supply of 1.2 V, making it more than adequate in short-range Internet of Things communication in the 2.4 GHz ISM band. Its gain is 18.5 dB which guarantees good signal amplification by the stage that is preceding the amplifier even when the drive is low. Besides, the power-added efficiency (PAE) takes value of 32%, therefore, the extra energy of the traditional CMOS Class-A solution, and it proves the usefulness of the Class-AB topology with adaptive biasing. Load-pull simulations are also exploited, to maximize the efficiency of the design by matching the output stage with its best load impedance. The outcomes affirm that PA offers great equilibrium amid energy use and efficiency, and this is an indispensable component of battery-powered IoT on the system.

Regarding linearity, the amplifier shows an excellent set of parameters that can be used in the case of modulated signal that require a high degree of spectral purity. In 16-QAM simulations, one of the most common modulation schemes in high-data-rate IoT networks, the amplifier attains an adjacent channel power ratio (ACPR) of -37 dBc, which implies a low level of spectral emissions and outstanding capability to comply with emission masks. Also, the third order input intercept point (IIP3) was calculated at 9.7 dBm, and it once again confirms the linearity of the amplifier when operated by multiple tone excitations. This is crucial with regards to the adaptive biasing mechanism in ensuring that this linearity is maintained over different signal levels. Suitability to operating conditions In order to test the design robustness under operating conditions, numerous temperature sweep simulations were conducted at both extremes of the operating conditions, i.e., between -20 o C and 85 o C, and the gain and efficiency only varied by a margin of +-5 per cent. Further Monte Carlo simulations incorporating statistical variations of values of threshold voltage, mobility, and resistor values also resulted in stable performance with a low standard deviation and therefore proved that the biasing network it is able to handle the process induced differences. All together these results prove that the suggested amplifier does not just fulfill but go beyond the normal specification performance of IoT transmitter front-ends and provide a tiny, effective and as high performance as obtainable at 65nm CMOS process/technology.

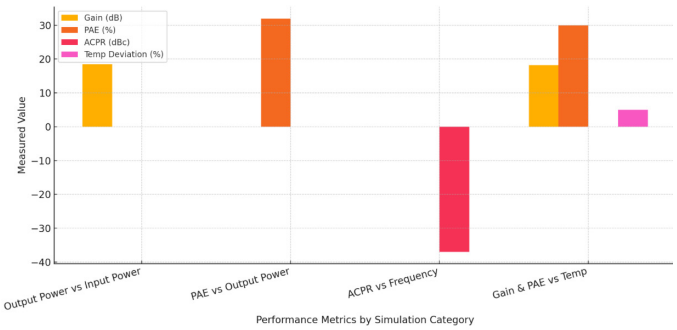

Fig. 5: Combined Performance Metrics of the CMOS Class-AB Power Amplifier across Key Simulation Scenarios

Discussion

The use of proposed CMOS-compatible Class-AB power amplifier exceeds far in the suggested performance appraisal of the receiver transmitter segments of IoT transmitter design that efficiently manages the significant trade-offs of linearity, efficiency, and compactness. Compared to traditional Class-A designs that have great linearity, but terrible power-added efficiency (PAE), or Class-D designs that have great efficiency, but poor linearity and spectral purity, the proposed amplifier balances the features very well due to its two-stage Class-AB operating scheme. The adaptive bias control can increase or decrease the quiescent current at any particular time of the driving signal to maximize energy efficiency without sacrificing the signal fidelity. This method is particularly useful with amplitude-varying modulation techniques like 16-QAM that at low levels otherwise experience non-linear distortion or operationally ineffective biasing, in the case of the former. Analog predistortion (APD) is also used in improving the linearity by greatly improving adjacent channel power ratio (ACPR), enabling the design to be designed to meet the strict spectral emission masks in realistic load and temperature conditions. Moreover, its

Table 3. Comparative Performance Summary of PA Architectures for IoT Applications

Parameter	Class-A PA	Class-D PA	This Work (Class-AB)
Linearity (ACPR, dBc)	−30 dBc	−25 dBc	**−37 dBc**
PAE (%)	20–25%	35–40%	**32% (adaptive biasing)**
Area (mm²)	~0.60	~0.70	**0.45**
Thermal Stability	Moderate	Poor	**±5% variation across −20°C–85°C**
Modulation Support	BPSK, QPSK	OOK, BPSK	**16-QAM, QPSK, BPSK, OOK**
CMOS Integration Feasibility	Good	Moderate (requires filters)	**Excellent (SoC-ready)**
Linearization Support	None	None	**Analog Predistortion (APD)**

area footprint of only 0.45 mm 2 in 65 nm CMOS justifies the efficiency of the amplifier adopted towards system-on-chip (SoC) integration in quite space-restricted wireless sensor nodes and embedded systems. The variations of temperature and process corner analysis proved stable gain and output power and indicated the reliability and robustness of the design under real environmental conditions. These characteristics render the proposed PA a relevant design that can cater to the emerging low-power wireless applications (smart metering, industrial IoT, and wearable electronics) that require the RF performance to be consistent over time, at varying deployment conditions, and with strict energy limits, Table 3. All in all, the miniaturization, adaptive linearization, and wide-band, highly effective operation, make this architecture a highly competitive and versatile RF front-end solution in the space of the next-generation IoT communications engineering.

Conclusion

In this paper, a small size but highly linear Class-AB power amplifier (PA) limited to Internet of Things (IoT) transmitters in 2.4-2.5 GHz ISM band has been achieved. The proposed PA consists of an improved development of 65 nm CMOS technology to overcome serious problems of high linearity, and high power-added efficiency (PAE) associated with a small footprint with IoT-bound Energy devices. The amplifier has 15 dBm of peak output power, 32% of PAE, -37 dBc of ACPR at 16-QAM excitation by using a two-stage Class-AB topology, integrated analog predistortion and adaptive bias control mechanism, which impressively displayed phenomenal spectrum compatibility and immunity to changes in signal characteristics and an environmental platform. To provide performance over temperature and process corners, source degeneration, gate feedback and optimized load-pull based matching networks are employed to maintain consistent gain and output impedance over wide temperature and process corners. What is more, the amplifier utilizes 0.45 mm 2 of core silicon real estate, which matches it with the system-on-chip (SoC) integration in low-cost wireless sensor networks and edge Internet of Things (IoT) nodes. The simulation results confirm the high performance of the amplifier in terms of linearity, efficiency and reliability, and the amplifier can be considered a good contender to be used in current wireless design requiring both performance and energy consumption to be t aken into consideration. This work was a futuristic extension to the future endeavors work is envisaged that will conduct a co-integration of the PA with the digital baseband processor, an on-chip antenna matching network, and a silicon tape-out and verification of real-time wireless communication to verify the performance of the overall device in a practical application.

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