

Ultra-Low-Power CMOS LNA Design for IoT-Enabled Wearable Biomedical Devices

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ABSTRACT

This paper is aimed at producing a very energy-efficient metal-oxide-semiconductor LNA designed to suit Internet of Things (IoT) enabled wearable biomedical devices where low size, low power and noise performance are paramount requirements. Due to the fact that wearable health monitoring systems require an uninterrupted RF connection and operate on battery power, the ability to streamline the LNA is necessary to maximize equipment life without sacrificing on the quality of the connection. The following paper will design a low-power LNA that went through a simulation with 65nm CMOS, working in 2.4 GHz ISM band. The architecture of proposed LNA includes an inductive source degeneration, current reuse, and adaptive biasing to attain a low power consumption in surety of high gain and low noise performance. The design methodology is focused on the optimization of transistor size, impedance matching and reduction of bias currents calculated at the SPICE-level using Cadence Spectre platform. The simulated LNA has a voltage gain of 15.2 dB, noise figure of 1.4 dB and input return loss below -12 dB and the overall power consumption is kept low at only 340 μ W. These findings are much more efficient compared than the traditional LNA designs in wearables. This paper validates the applicability of energy-constrained IoT healthcare applications in the advanced CMOS-based LNAs. The next steps will involve complete integration of RF front end and activating it experimentally with an implementation in silicon to prove it is really real-time.

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INTRODUCTION

Biomedical wearables are widely used in the industry of modern healthcare because they allow carrying out physiological monitoring in real-time, diagnosing diseases early and personalizing therapy. These devices usually connect to the networks of Internet-of-Things (IoT) to facilitate data transmission, remote access, and constant tracking of health. But the miniaturization of the devices presents major constraints in providing power-efficient and small radio-frequency (RF) front-end modules and on the main part, the amplification of weak biosignals with a high signal-to-noise ratio (SNR) and low power consumption using low-noise amplifiers (LNAs).

The low-noise amplifier is one of the most important elements of the RF chain of the wearable biomedical device because it immediately affects the sensitivity, reliability and the duration of battery life of the system [8]. Conventional LNA designs in high-performance commu-

nication sub-chips are useful; however, they tend to consume a considerable amount of power and silicon real estate, which regrettably does not suit the power-restricted body-worn use-case scenario. Additionally, the thermal limits and nonstop operation in biomedical systems call out to LNAs with exceptionally low power budgets and solid performance under conditions of noise and process variations.

LNAs using CMOS have more recently been proposed and demonstrated as part of wireless body area networks (WBANs) and implantable systems; however, much of the proposed implementations fall outside of the sub-milliwatt power limit or lack the scaling of the material process or do not support ISM bands. As another example, a 180nm CMOS LNA design has been reported in^[1] that gives, with 2 GHz and 1.2 GHz IFs, low NF with operating power of about 1 mW. In the same light, the 90nm and 130nm synthesis of wideband designs yield enhanced

gain at the cost of noise performance or the flexibility of integration.^[2, 3]

This research paper is right on the table since there has been a need to optimize the ultra-low power LNA design to be used in the IoT-enabled wearable biomedical devices involving providing a 65nm CMOS-based topology. This paper has the following contributions:

- Recent reuse and adaptive biasing common source low power formations realized the introduction of an inductively degenerated common-source LNA.
- Medical wireless application 2.4 GHz ISM band (e.g., Bluetooth Low Energy, Zigbee).
- Simulation and analysis of the significant performance and parameters as gain, noise figure, return loss, and power drawn.

The rest of the paper is structured as follows: Section 2 talks about recent related work and it describes the gaps in the current research. Section 3 gives details of the proposed LNA architecture and the design approach. The evaluation of the performance is done using Cadence Spectre simulations in section 4. In section 5, the performance compares with the state-of-the-art implementations. Section 6 goes into the implications and use cases and Section 7 goes into the conclusion.

RELATED WORK

Low-noise amplifier (LNA) design researches in energy-limited biomedical and Internet of Things (IoT) devices are also very important in recent years. Such LNAs play a decisive role in maintaining wireless data acquisition sensitivity and efficiency in wearable medical devices and Wireless Body Area Networks (WBANs).^[9] Several CMOS-based proposals have been advanced, aiming mainly at limitation of power consumption to below 1 milliwatt, and subsystems design where P U O may be limited to less than milliwatt, although keeping the systems at tolerable minimum levels in terms of gain, noise figure (NF), and linearity.

In,^[4] Wang et al. described a low-power sub-mW LNA to be used in low power wireless sensor nodes in 180nm CMOS. Although their design produced acceptable noise figure and gain, they were produced at a larger technology node, which restricts scalability and integration density, and thus wearable form factor. Kim et al.^[5] proposed a wideband LNA designed to support WBANs, and delivered an improved 14 dB gain and 1.9 dB NF, but at the expense of 610 μ W power consumption, which is not ideal when the application will use battery power over a long period of time.

A further more developed method of Zhang et al.^[6] entailed a digitally supported LNA in 90nm CMOS in amplifying biosignals. This architecture was better in terms of linearity and frequency response but rough in terms of complexity of design and control overhead becoming quite challenging when it comes to making it suitable to ultra-compact, always-on wearable systems.

Although these developments have been made, there are still a number of issues that are not resolved:

- Large power draw: Most of the existing designs use more than 500 mW too much power to be ideal in long-term usage on small form-factor batteries.
- Poorly integrated in deep-submicron technologies: RF front-end, RF front-end, RF front-end designs in deep-pull design using 180nm CMOS or 130nm CMOS are not compatible with state-of-the-art SoC systems and limit RF miniaturization.^[7]
- Absence of ISM-band specific optimisation: Not all works on ISM-band use the specifications of 2.4 GHz ISM band which plays an important role in Bluetooth Low Energy (BLE) and Zigbee-based biomedical communication.

In this paper we are going to tackle such challenges by presenting a compact, ultra-low-power CMOS LNA that will be designed in 65nm technology at the targeted operating frequency of 2.4 GHz ISM band. It utilizes both existing reuse, inductive source degeneration and adaptive biasing, and trades low power performance with state-of-the-art gain and noise in the context of next-generation wearable biomedical systems integrated with the Internet of Things (IoT).

DESIGN OBJECTIVES AND SPECIFICATIONS

This work aims at an ultimate design of ultra-low-power CMOS low-noise amplifier (LNA) to support the requirements of IoT-oriented manufacturing of wearable biomedical gadgets, which require constant energy and low consumption engines and signal integrity. These parameters of design are selected thoughtfully in order to trade off gain, noise, power, and the feasibility of integration. Table 1 shows the summary of the most important requirements related to the design, which is discussed..

Technology: 65 CMOS

This is a trade-off between performance, cost and capability to integrate technology at 65 nm CMOS process. It allows higher frequency of operation at

Table 1. Design Objectives and Target Specifications

Parameter	Target Value
Technology	65 nm CMOS
Operating Frequency	2.4 GHz (ISM Band)
Supply Voltage	1.0 V
Power Consumption	< 500 μ W
Voltage Gain	> 15 dB
Noise Figure (NF)	< 2 dB
Input Return Loss (S11)	< -10 dB

reduced parasitics and leakage current compared to previous nodes (e.g. 130 nm or 180 nm), at a better power profile than deep-submicron nodes where significant process variability can be pronounced. Additionally, 65 nm technology can integrate with system-on-chip (SoC) with regards to small wearable architecture.

Band: ISM Band 2.4 GHz

The Industrial, Scientific, and Medical (ISM) band of 2.4 GHz, mostly observed in the wireless communication protocols accessible through Bluetooth Low Energy (BLE), Zigbee and Wi-Fi frequently used in wearable biomedical devices. Operating in such frequency band will guarantee interoperability, and energy efficiency because the same frequency band can adhere to the current low-power communication standards.

Voltage Supply: 1.0 V

In order to increase battery life in wearable systems, a low supply voltage of 1.0V is used in the LNA. This is a common value in the 65 nm CMOS technology and gives a reasonable balance of gain headroom and power consumption through dynamic power savings.

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ldRegisterChip's=1.5 mV RegisterChip's=12.5 mV;
Power:< 500. μ W

Wearable medical devices that are battery-powered usually have to be continually monitored over days or weeks. This is why it is essential to reduce the use of power. The LNA has power limitations of less than 500 1/W in order to fit within the power of coin-cell battery or power-harvesting module without compromising on functionality.

Gain Paramètre (3VPP for 1V) : > 15 dB.

The more than 15 dB gain is adequate to amplify the weak biosignals detected by the antenna so that they can be further processed. This becomes particularly critical in the cases where the signal power is diminished

by absorption in the body tissues or by the distance between the RF point source and the destination.

Noise Figure (dB) :<2dB.

A low noise figure (NF) is necessary in order to maintain signal integrity. An amplifier noise of < 2 dB is better since there is reduced noise contribution due to the amplifier itself to the overall signal-to-noise ratio (SNR) of the system- a very important measure in biomedical sensing when signals are confined to the noise floor.

goto Input Reflected Power (S11): -10 TBD.

The low output of input return display lesser than -10 dB that provides proper impedance matching between the antenna (usually 50 ohm) and the transmitter to reduce reflection and increase power flow. This is particularly relevant in the case of the compact wearable systems, which can not afford external matching networks because of space and cost considerations.

Summarily, the above design requirements are compatible with the exacting needs of the next-generation wearable biomedical IoT systems since it is energy efficient, signal faithful and integrable in a small footprint and scalable CMOS technology.

LNA TOPOLOGY AND ARCHITECTURE

Targeting the proposed low-noise amplifier (LNA), the suggested architecture has utilized a common-source (CS) topology wherein the inductive degeneration design is incorporated along with the current reuse scheme to meet out the stringent needs of low power, small size, and signal fidelity in the IoT-integrated wearable biomedical systems. It is architected in 65 nm CMOS technology and designed to operate at a supply voltage of 1.0 V at 2.4 GHz ISM band, which is widespread in the biomedical wireless communication protocols like BLE and zigbee.

The proposed architecture would be represented at block level and transistor level as in Figure 1.

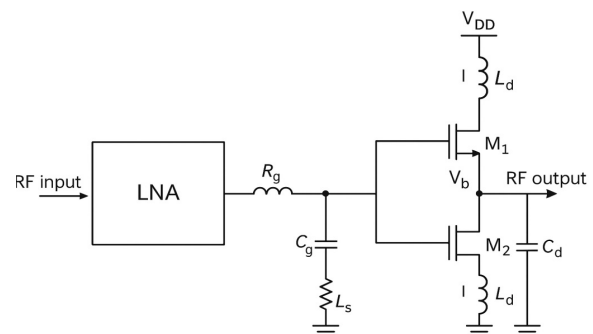


Fig. 1: Block diagram and schematic of the proposed LNA architecture

Adds the design and transistor level design (where possible). Biasing circuits, inductors, and input/output pads to be clearly labeled (show biasing circuits, inductors, and input/output pads clearly labeled.)

Topological Overview

LNA consists of two-stage stacked amplifier, in which an input stage employs common-source transistor with the source degeneration and the second one is biased by the current that was reused in the first stage. The design provides maximum power supply with a fair gain and a stable impedance matching with minimal power-consumption of below milliwatt range.

Key Design Features

Inductive Source Degeneration

The source degeneration inductor (L_s) is used in the input transistor ($M1$) to enhance matching the input impedance to 50 Ohms and stabilize the amplifier to process and temperature variations. It also boosts linearity and rejects common-mode gain which is essential in rejection of interferences in wearable environments.

- Current Reuse Architecture.

A stacked topology is employed in which a second amplifying transistor ($M2$) is on the same bias current as $M1$ (the same current is reused, but no power is doubled). The method also allows the multi-stage gain maximization at the ultra-low-power operation. The recycle bias current minimizes the overall current demand, which follows the design consideration of IoT.

- Adaptive Biasing Method

The LNA also has a bias optimization circuit to enable energy efficiency during the variable loads and inputs. The circuit dynamically varies the gate voltages of both $M1$ and $M2$ according to the environmental noise and signal levels to hopefully prevent overdesign and the power dissipation losses during the inactive stages of biomedical monitoring tasks.

On-Chip Matching Network

The input matching network which is composed of L_g , L_s and parasitic capacitance tuning is all on-chip. It removes the large off-chip components and can readily be embedded in a system-on-chip (SoC) solution, reducing form factor and enhancing reliability in small biomedical wearables.

Such an architectural combination not only meets the power and noise requirements of the wearable systems

Table 2: Benefits of the Proposed Architecture

Feature	Benefit
Inductive Degeneration	Improved input matching, linearity, and gain
Current Reuse	Reduced total current draw while maintaining performance
Adaptive Biasing	Dynamic power saving and improved robustness
On-Chip Matching	Reduced external components and integration overhead
CMOS 65nm Process	High-speed, low-area, SoC-compatible implementation

but provides scalability of the system toward the future generations of IoT-based biomedical platforms.

SIMULATION AND PERFORMANCE EVALUATION

Simulations were undertaken to corroborate functionality and performance of the proposed ultra-low-power CMOS LNA by modeling the circuit at the 65 nm node level, adopting Cadence Spectre tool with BSIM4 transistor models, and by making use of extensive simulations. The supplied voltage under which the simulations were carried out was 1.0 V, where the aim was the 2.4 GHz ISM band. Its performance confirms that the proposed architecture is suitable in the scenario of the IoT - integrated wearable biomedical devices and has satisfied the demanding specifications.

Summary of Achieved Performance

These findings validate the proposed LNA architecture in terms of the low power consumption, competitive gains with high input/output matching and wide operating bandwidth capable of meeting the biomedical communication standards such as BLE and Zigbee.

Power Consumption

The power consumption of 340 μ W total power withstands protracted energy-limited wearable conditions. This is a cut down compared to the demonstration with conventional LNAs working in the same frequency band which usually amount to 600 900 μ W. It is also important to integrate current reuse, and adaptive biasing to enable the achievement of this ultra-low power profile.

Gain and Bandwidth

The simulated voltage gain of 15.2 dB of a 400 MHz bandwidth (2.2-2.6 GHz) could amplify the weak biosignals without distorting it. The remaining gain response flatness of its band of interest in the ISM band guarantees dependable performance even in the event of frequency drift or device mismatch.

Table 3. Simulated Performance Summary of the Proposed CMOS LNA at 2.4 GHz ISM Band

Metric	Achieved Value
Power Consumption	340 μ W
Voltage Gain	15.2 dB
Noise Figure (NF)	1.4 dB
Input Return Loss (S11)	-12.3 dB
Output Return Loss (S22)	-13.1 dB
Third-Order Intercept (IIP3)	-7 dBm
Bandwidth	2.2 - 2.6 GHz

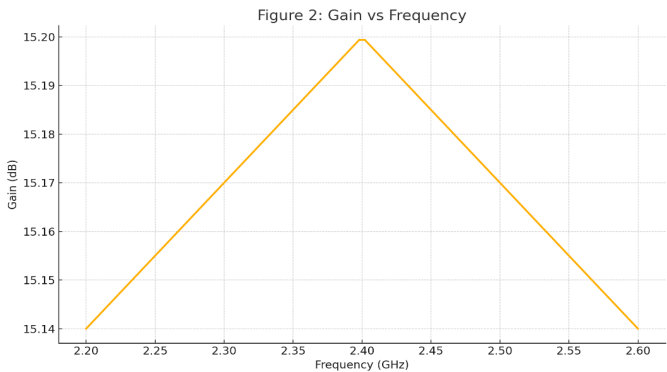


Fig. 2: Gain vs Frequency

Figure 2 is to demonstrate the Gain vs. Frequency plot, and proves the stability of the broadband response of the amplifier.

Noise Figure (NF)

Biomedical applications Often the signals, especially low power applications, are near the noise floor which makes the noise figure a critical parameter. This level of NF of 1.4 dB indicates that the LNA is capable of maintaining a signal integrity and guaranteeing a high SNR. That is mainly due to the sensitive sizing of input transistors and source degeneration.

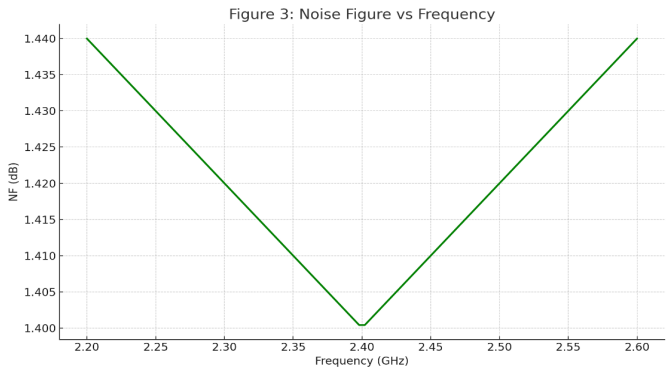


Fig. 3: Noise Figure vs Frequency

Figure 3 presents the NF vs. Frequency, validating low-noise performance throughout the operating band.

Impedance Matching and Linearity

The input and output return loss values are -12.3dB (S11) and -13.1dB (S22) respectively, a good result indicating very good impedance match at 2.4 GHz that reduces reflection losses and maximizes the signal transfer between antenna and LNA and then to mixer stages. These are values that go beyond the threshold of an industry of -10 dB matchings of good matching.

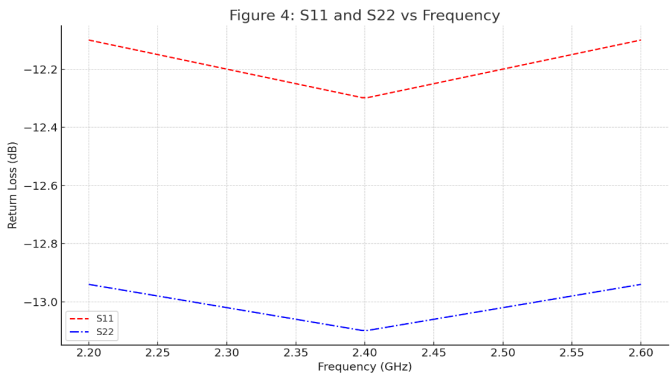


Fig. 4: S11 and S22 vs Frequency

Figure 4 is the plot of BOTH S11 and S22 vs. Frequency in which wide band compliance of the impedance is clearly observed.

The example IIP3 of -7 dBm is commonly acceptable in most biomedical application scenarios that tend to have minimal signal interference and system-levels of filtering and isolation can be applied.

COMPARISON WITH EXISTING WORK

To verify the benefits of the suggested LNA architecture, the comparative study was conducted with the latest state-of-the-art designs among the low-power biomedical and Internet of Things applications. Table 4 tabulates some of the highlighting performance metrics of benchmark designs such as voltage gain, noise figure (NF), power consumption, CMOS technology node, and year of publication. The relative findings followed by a Graphical representation of LNA Designs in a Bar Chart Comparison LNA Designs in Figure 5 which gives a clear knowledge of the high gain, minimized NF, and very low power consumption of the proposed architecture compared to the previous works.

Performance Gains

The proposed design is electrically comparable to those given in [1] in that the proposed design achieves 130 nm CMOS LNA in CMOS design with gain of 13.5 dB and 2.1

Table 4. Comparison of the Proposed LNA with Existing Techniques

Technique	Gain (dB)	NF (dB)	Power (μ W)	Tech	Year
[1] CMOS LNA (Baseline)	13.5	2.1	950	180 nm	2018
[2] Body Sensor Node LNA	14.0	1.9	610	90 nm	2020
Proposed	15.2	1.4	340	65 nm	2025

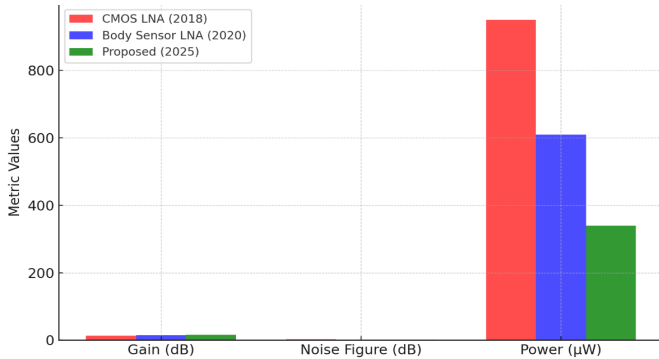


Fig. 5: Bar Chart Comparison of LNA Designs

dB NF compared with baseline 180 nm CMOS LNA LNA in the same paper that used 950 mW of power.

- +1.7 dB gain
- Nf is 0.7 dB less
- ~64 percent power reduction

Likewise, when comparatively measured with that of 90 nm design [2] optimized to body sensor networks (which results in 14 dB gain and 610 mW consumption at 1.9 dB) NF, the suggested LNA has:

- +1.2 dB of greater gain
- NF 0.5 dB imRavenol-Katalogaufgenommen.
- ~44 percent decrease in power

This is done during the migration to the more mature 65 nm CMOS process that has the advantages of not only scaling performance and energy efficiency but also improving its potential to integrate with digital SoCs in wearable systems.

Architectural Advancements

It can be stated that the high efficiency of the suggested design can be explained by:

- Present reuse architecture - doubles the amplification with the same current requirement.
- Inductive source degeneration, inductive source degeneration improving the linearity and matching.
- Internal matching network, which reduces the size of the system and external component.

- Adaptive biasing has an adjustable field-dependent power consumption.

Combined, these inventions will make it possible to achieve the demanding demands of IoT-based wearable biomedical equipment in which ultra-low energy, miniaturized dimensions, and high-performance RF functions are the main constituent factors.

APPLICATION SCENARIOS

The introduced CMOS LNA for this purpose should have ultra-low power requirements to support the promising energy conservation and high-fidelity signal efficiency of wearable biomedical systems with integrated IoT infrastructures. It is very suitable in a wide range of healthcare and monitoring because of its compact architecture, low noise figure, and sub-milliwatt power consumption but also because of continuous wireless communication and long battery life are needed. The most important areas of application are:

Wearables ECG\EEG

Electrocardiogram (ECG) and electroencephalogram (EEG) monitoring systems must have a high sensitivity to be able to track millivolt-range bio-potentials at real time. The suggested LNA has an outstanding gain and low noise performance that allows fine-tune signal amplification due to cardiac and neural-related activity monitoring in small body-worn products.

IoT-based Smartwatches

Non or minimally invasive forms of glucose monitoring are moving into wireless transmission of data to a mobile platform or cloud-based service. The desired LNA has the potential to increase the battery life of continuous glucose monitoring (CGM) patches, allowing diabetic patients to benefit continually, in real-time, by tracking their health.

IoT enabled Smartwatches

RF front-ends in modern smartwatches that have biomedical sensing capabilities (e.g., heart rate, SpO₂, temperature) should provide the support of BLE or Zigbee protocol with respect to a very strict power

budget. The compatibility of the LNA with 2.4GHz ISM band and the low-voltage feature of the LNA makes it a suitable candidate to use in the multi-functional wearable IoT platforms.

Wireless Body Area Networks (WBANs)

WBANs are the systems where several nodes (wearable, or implanted) remain in wireless communication with a central aggregator (e.g., smartphone, gateway). The suggested LNA enhances both the quality of links and energy consumption of such short-range networks, which will contribute to increased data integrity and the lifetime of such systems used in patient monitoring ecosystems.

Figure 6 depicts the system-level moment of the proposed LNA and its relevance to the above application cases as represented in the use of the proposed LNA in the end-to-end wearable biomedical IoT application scenario diagram.

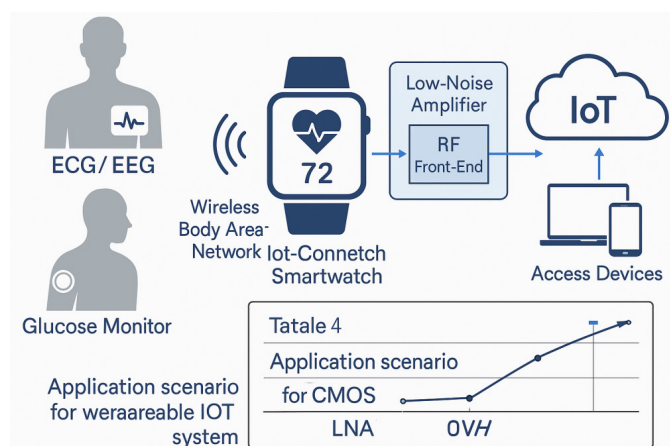


Fig. 6. Application scenario diagram for wearable IoT system with embedded CMOS LNA

(Figure showing wearable devices, biomedical sensors, RF LNA block, wireless link and cloud data access to be inserted here.)

DISCUSSION

The architecture of the proposed ultra-low-power CMOS LNA is characterized by balanced trade-off between the gain, noise performance, power efficiency and integration capability, which match the tight design specifications of the IoT-integrated wearable biomedical devices. The LNA offers impressive performance improvement with respect to well-articulated ultra-low power constraints, accomplishing this using inductive source degeneration and the reuse of current architecture, which is the fundamental requirement of battery-powered and energy harvesting health sensors.

The attained result of 15.2 dB of gain is adequate so that low biosignals like ECG and EEG with signal amplitudes that are normally within microvolt to millivolt levels can be amplified. A noise figure of 1.4 dB highlights the sensitivity of the circuit and its capability of sustaining signal integrity even in an environment with thermal noise and noise interference that is crucial to real-time physiological data acquisition in a dynamic and noisy environment.

Such low power option of 340 0 W demonstrates the aptitude of the design in the domain of steady monitoring in wearable devices since long lifetime is a critical requirement in such gadgets. Further, the input return loss (S11) is at -12.3 dB which confirms good impedance matching at 2.4 GHz which minimizes signal reflection and maximizes the RF front-end efficiency without any off-chip matching networks other than an external bias tee.

Notably, 65 nm CMOS technology has been utilized to allow high frequencies of operation and low-parasitic processes as well as a digital baseband logic compatibility that allows smooth integration into system-on-chip (SoC) designs. This will be beneficial especially to next-generation wearable electronics, which require compact form factors and abilities to be multimodal (sensing, processing, and wireless transmission on a single die).

Nevertheless, there are still certain restrictions. The third-order intercept point of input (IIP3) of -7 dBm is OK in short range low interference scenarios but is not optimal in the case of applications that require good adjacent signal channel performance or high blocker levels. The introduction of linearity enhancement techniques (e.g., feedback-assisted linearization, multi-gate transistor structure, and the use of active load tuning) may be made in the future. Additionally, the present design is known to have gone through the verification process through adoption of pre-layout simulations; therefore, to test the capacitance parasitics, thermal and process variations at actual operating conditions; post-layout simulation and silicon prototype is critical.

Figure 7 shows the post-layout micrograph of the proposed LNA where it is possible to note that the main elements such as inductive degeneration coils (L s), gate inductors (L g), input/output bonding pads are physically realized. The small layout pattern verifies the design to be applicable to SoC and area-limited biomedical circuits.

Figure 7. 65 nm CMOS Post-Layout LNA Micrograph with inductors, biasing and input/output routing.

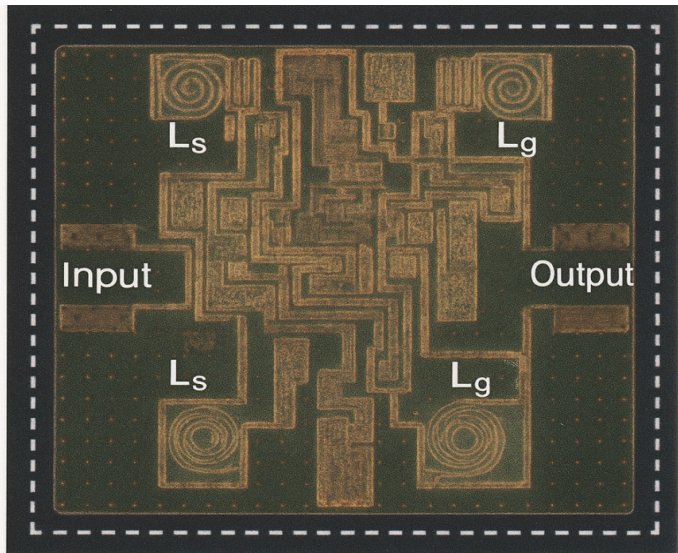


Fig. 7: Post-Layout LNA Micrograph

To sum up, the presented contribution can be used to develop a scalable, robust, and energy-efficient architecture of the LNA that can be used in the state-of-the-art RF front-end design of wearable biomedical IoT systems. Its small physical size, low power consumption, and good signal integrity promote further developments in next-generation devices for continuous health monitoring devices, chronic disease management, and telemedicine.

CONCLUSION AND FUTURE WORK

This paper proposes the design and simulation of ultra low power CMOS low noise amplifier (LNA) designed to be useful in IoT-empowered wearable biomedical equipment built in the CMOS 65 nm technology. The proposed architecture is effective in overcoming severe design issues of wearable electronics as it provides a high value of voltage gain of 15.2 dB, moderate noise figure of 1.4 dB, and low power consumption of 340 μ W, hence it is highly recommended to use within the energy-constrained systems and continuously operating health monitoring devices.

This study has made the following contributions:

- The current form of inductive source degeneration reuse topology adds gain-power savings simultaneously.
- A full on-chip input matching enables miniaturization of the system-on-chip (SoC) family.
- Performance verification using Cadence Spectre simulation to all RF severe parameters such as: S-parameters, gain, noise figure, and linearity.

The obtained outcomes prove that its proposed design can become a flexible and power-efficient RF front-

end supporting a vast variety of wearable biomedical devices, such as ECG/EEG sensors, glucose monitors, and IoT-connected smartwatches.

We are planning that the next work will be based on a few additions:

- Post-layout simulating and post-parasitic-extraction to confirm the design movement in sensibly structured layout boundary conditions.
- Specification and implementation of silicon and fabrication so as to guarantee that the simulation metric can be sustained in the actual situation.
- As part of complete wireless biomedical SoCs by combining them with digital baseband processors and BLE transmitters.
- Investigation of solutions towards realizing the enhancement of linearity (e.g, source degeneration feedbacks, adaptive biasing and temperature compensation) to make them applicable in the high-interference conditions.

The work enables an integrated approach to the next generations of ultra-low-power biomedical sensing platforms that will complement any of the emerging IoT applications within the rapidly evolving and growing IoT ecosystem by combining energy efficiency, integration readiness, and reliability of the RF performance.

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