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RESEARCH ARTICLE

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Design and Optimization of a Wideband Low-Noise Amplifier for 6G mmWave Applications

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Abstract

The even speedier advance of sixth-generation (6G) wireless communication systems requires the creation of high-performance millimeter-wave (mmWave) radio frequency (RF) front-end components that have the ability to work against large bandwidths with a greater gain and noise performance. Low-noise amplifier (LNA) is one of these elements providing that the overall sensitivity of the receiver chain, as well as the fidelity of the signal is largely dependent on it. The following paper illustrates the design and optimization of a Wideband LNA centered at mmWave 24-40 GHz band that contains several key 6G communication channels such as 28 GHz and 38 GHz bands. The advanced LNA architecture is a multi-cascade architecture with the source degeneration technology and inter-stage LC matching networks to bring the appropriate compromise between gain, noise figure (NF) and bandwidth. This design uses the 65nm CMOS technology that offers a low cost chip and supply of scalable integration into the new generation wireless systems. The main performance parameters consist of best gain of 21.8 dB, minimum NF of 2.5 dB and input reflection coefficient (S11) less than -10 dB throughout the whole L-band of 16 GHz. Resistive loading and feedback methods are used, and the stability is guaranteed up to the operating band. Schematic-level simulations are run with Key sight Advanced Design System (ADS) to achieve robust design as well as EM layout-aware simulations with CST Microwave Studio to achieve layout feasibility. The layout and package interactions have also been considered, and the design is able to take into account the effects of layout and package interaction through parasitic-aware modeling. The proposed LNA, due to its optimized performance footprint of the layout, energy consumption, and suitability for 6G-based mobile devices, small cell base stations, and IoT hubs is likely to be embedded with ease. This paper brings to the table a validated and feasible implementation methodology of wideband mmWave LNA design and establishes a platform on how the RF front-end will be integrated in more advanced 6G communication platforms.

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Introduction

The need to develop the sixth-generation (6G) wireless communication systems has fueled the desire of having highly and efficiently integrated radio frequency (RF) front-ends systems to be used to support the new radar wideband and the emerging radio communications in radar systems which is likely to operate reliability at millimeter-waves (mmWave) frequencies. As 6G is projected to support higher data rate, sub-nanosecond latency, and connect billions of devices and the RF front-end module is projected to be required to take into account even more strict performance parameters over broad bandwidths, namely, 24-40 GHz. These bands at this frequency range are some of the most important ones in the 6G bands, including 26 GHz, 28 GHz, and 38 GHz, and essential applications in high-speed mobile broadband, communication of Internet of Things (IoT), autonomous vehicles, and immersive experiences of XR.

One of the most important components in any radio frequency (RF) receiver system is the low noise amplifier (LNA), the job of this component is to strengthen weak signals that are received into the receiver and at the same time not to add excessive noise to the system. In Figure 1, sensitivity and dynamic range of the whole

receiver are directly related to the performance of the LNA. In the case of mmWave applications, however, the design of LNA becomes much more difficult because more and more influence is caused by the parasitic elements, layout-induced losses and the very limited quality factors (Q) of the passive components and the non-repeatable process variability of CMOS process at high frequencies. Besides, impedance matching of the broadband impedance over a wide frequency band is not a trivial problem, because gain and noise figure (NF) are potentially sacrificed in the process.

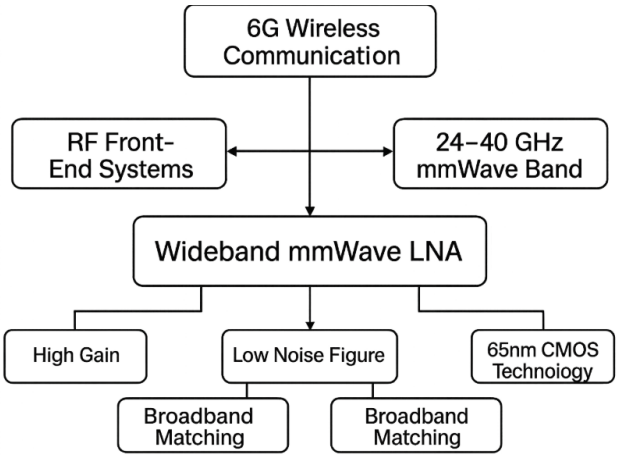

Fig. 1: Conceptual Overview of a Wideband mmWave LNA for 6G RF Front-End Applications

To overcome these hurdles, it is necessary to use innovative design methods of LNA such as multi-stage topologies, using source degeneration to optimize the noise figure, and employ use of inter-stage matching networks to provide broadband gain-related improvements. Additionally, low-power, small size and affordable realization requirements work in favor of deep submicron CMOS technologies, although with their of course adverse characteristics of gain and noise at millimeter waves.

This paper gives design and optimization of a wideband LNA having 24-40 GHz band with 65nm CMOS technology. The suggested LNA adopts a cascoded multi-stage, source degeneration and LC matching to attain wideband input matching, low NF and high gain. It uses simulation tools like the Key sight ADS and CST Microwave studio to validate performance, and through layout-aware modeling, there is accurate prediction of the physical behaviour. The architecture is intended to be embedded in mobile platforms enabled by 6G, smart infrastructure with a balanced set of performance, efficiency, and scalability. The study would provide the valuable design methodology toward the development of mmWave LNA, and it would assist in the development of the next-generation wireless application that would be energy efficient.

Related Work

In recent years, great interest has been devoted to the development of low-noise amplifier (LNA) design to mmWave. Indeed, this topic has been actively pursued especially in the wake of the uptake of 5G and the foreseen demands of 6G communication[6] systems. A variety of CMOS and III-V, semiconductor-based implementations have been developed to address the needs of high gain, low noise and wide bandwidth at mmWave frequencies.

In,[1] a single-stage cascode topology (source-degenerated) 28 GHz LNA based on a 65nm CMOS technology was reported. Despite the low noise figure (NF) and gain of 3.2 dB and 19 dB respectively, the overall[8] bandwidth was extended to only 4 GHz which does not support large-scale broadband 6G applications. The paper in[2] provided, in turn, a 38 GHz application focused high gain LNA in[9] GaAs pHEMT technology which has better linearity performance, but at greater cost and reduced potential integration with digital CMOS components.

Ways to meet this requirement of broadband operation include a three-stage distributed amplifier architecture that was proposed by[3] and[10] which operates over a range of 20-40 GHz.[11] The design had the problem of power consumption and silicon area multi-wide[12] matching networks were used. In,[4] a different form of inter-stage matching based on transformers was used to increase the bandwidth whereas the compactness of[13] was preserved and inter-stage matching provided a way to have good insertion loss characteristics, but inter-stage matching based on on-chip transformers constrained the gain and worsened noise figure.

In more recent research,[5] showed a dual-path[14] LNA in 28nm CMOS which had a high- gain and a low-gain path which were switched according to the input conditions to provide optimum power consumption.[15] Although this method yielded more energy efficiency, it brought complexity in control as well as non-linear under a high-input power environment.

On the whole, the earlier literature has played a major role when it comes to the compensations of performance in respect to gain, NF, and linearity. Nevertheless, there is a need to find a gap in a simultaneous delivery of wideband input matching, low NF, high gain, and rugged operation under process-voltage-temperature (PVT) variations in the design of LNAs by the use of standard CMOS technology. This research can fill these gaps since it reports a multi-stage, broadband LNA implemented in 65nm CMOS, with compact on-chip matching networks,

optimized at 2440 GHz range, corresponding to the requirements of 6G mmWave communication system.

LNA Design Architecture

Frequency band and Technology

The targeted wideband low-noise amplifier (LNA) is specifically made to work with the 24 40 GHz frequency range which contains most significant mmWave assignments that are 6G communications is to be made with, such as the most prominent 28 GHz and 38 GHz frequencies. Such frequency bands are essential ro supporting ultra-high data rates applications like: Holographic communications, immersive XR, and machine-type interaction at real-time in wireless future networks. A 65nm RF CMOS process is then used to implement the LNA to achieve the extreme performance requirements attainable at these higher frequencies, providing an attractive balance between high frequency performance, low power and integration capability. This decision is based on the need to achieve RF solutions in a low-cost, scalable, and digitally compliant manner and with a view toward large-volume integration in mobile and IoT devices. CMOS has proven to be a viable candidate at these mmWave frequencies despite several drawbacks including inferior gain (which implies that signal amplitudes are lower at a given frequency), as well as higher parasitic effects than either GaAs or SiGe. Such limitations are effectively overcome through good device sizing, matching network optimization and layout-sensitive parasitic modeling considerations. The supply voltage of 1.2 V is used to optimize both transistor performance and power-efficiency in applications where the amplifier is required to have adequate headroom on multi-stage amplifier topologies with low power consumption. As shown in figure 2 this voltage level also is compatible to standard CMOS nodes and thus can be integrated with mixed-signal and digital baseband. On balance, the chosen frequency range and technology to implement the process will serve as the optimal basis to create a high-performance, wideband LNA in the context of the demands of the 6G mmWave front-end architectures.

Topology

The wideband low-noise amplifier (LNA) is proposed as a multi-stage cascode architecture with a particular feature of achieving the desired high gain, wideband input matching, and strong reverse isolation of the receiver within the proposed device, as essential parametres of effective mmWave front-end functioning in the system of

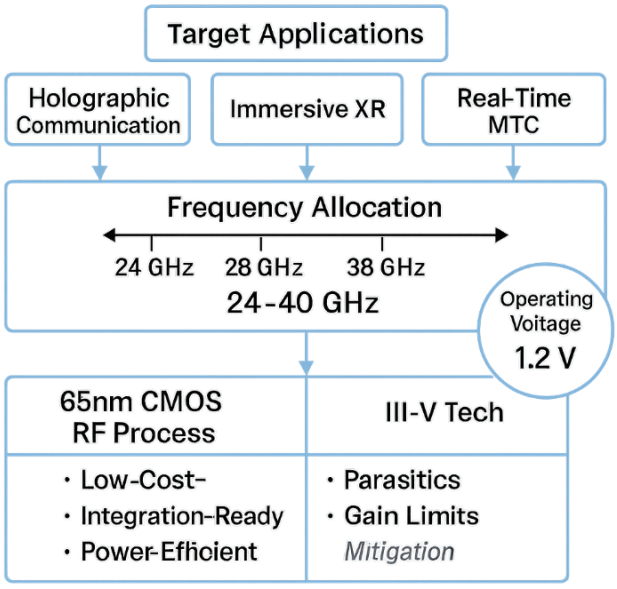

Fig. 2: Technology-Frequency Mapping and Application Relevance for 6G mmWave LNA Design

6G. The core of the architecture is a cascode input stage that represents a common source transistor coupled with a common-gate transistor. This configuration is also not only a great voltage gain programmer raising the output impedance, but also gives superior reverse isolation, thus contributing to the minimisation of unwanted feedback, and resulting in superior amplifier stabilisation. In order to provide broadband in matching the input to broadband, source degeneration has been used on the input transistor by employing an appropriately sized inductor. The technique flattens the real part of the input impedance and facilitating noise matching in the operating bands allowing a reduction in noise figure (NF). Inter-stage LC resonators are used between gain stages to give impedance transformation and peaking at specific frequencies to enhance gain flatness and out of band noise suppression. The resonators are modeled in a precise electromagnetic modeling fashion to include parasitics and process variations so as to have robust performance under realistic operating conditions. Also, on-chip bias generation circuits are integrated into the design to achieve fixed and temperature-independent biasing which is very important to the continuous amplifier performance across changing environments. Input and output nodes (handling and packaging) are also designed with electrostatic discharge (ESD) protection circuitry to help protect the LNA, and avoid much parasitic loading. Figure 3 The combination of this topology has an optimal balance between performance of high frequency gain, the input matching bandwidth, the noise characteristics, and integration capabilities and is therefore an ideal choice of 6G-enabled CMOS RF receiver development.

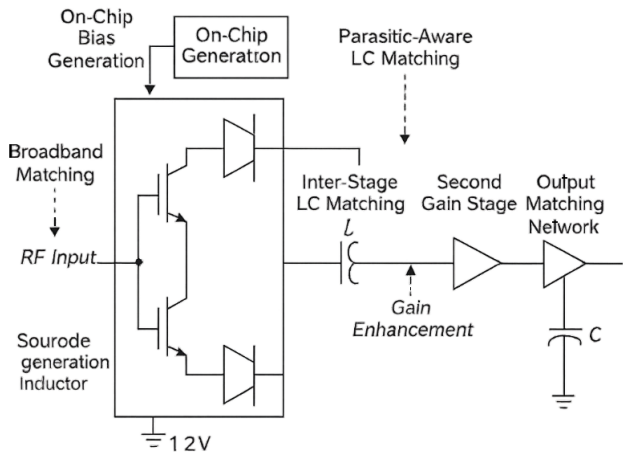

Fig. 3: Block Diagram of the Proposed Multi-Stage Cascode LNA Topology for 6G mmWave Applications

Design Methodology

Schematic Design

The proposed wideband low-noise amplifier (LNA) is carefully designed on the schematic- level to ensure optimisation of the gain and noise characteristic, linearity and stability as it tries to remain within the boundaries of the 65nm CMOS technology at mmWave frequencies. The size of transistors in any stage is calculated by utilizing the gm/ID design approach that is common due to its effective tradeoff between gain, power consumption, and speed. The method helps designers pick the best inversion level of MOSFETs whereby there is the precise ability of controlling Tran's conductance efficiency (gm/ID), directly affecting the available gain and noise figure. The design has high gain and yet does not cause large power use by aiming at moderate to strong inversion of input transistors and cascoding devices.

The input transistor is also biased in the vicinity of the optimum noise point, which puts the noise figure (NF) at a minimum, with the optimum noise point lying at some value of gate-source voltage with the minimum amount of thermal noise contribution. The source degeneration inductor is also co-optimized with transistor dimensions so that the optimum noise impedance match is obtained, and the bandwidth of the input match is also improved. Electromagnetic modeling and layout-sensitive parasitics extraction are used to make accurate choices of high-Q on-chip inductors and capacitors, suitable for and used in post-layout designs as part of the matching and degeneration networks.

To have absolute stability across whole operating frequency range and under all process-voltage-temperature (PVT) corners, both series and shunt feedback networks are usable. The series feedback is used to enhance linearity and gain control of the input impedance, whereas feedback is usually used in shunt from a resistor or capacitor to quench any oscillations and to increase reverse isolation. The feedback paths are well dimensioned, to ensure there is a K-factor greater than one and any gain peaking there may be out of band is suppressed. Figure 4 In general, the schematic design approach has satisfied that the amplifier has high performance characteristics under formidable 6G standards with reliability and repetitiveness and a margin in the real-life implementation.

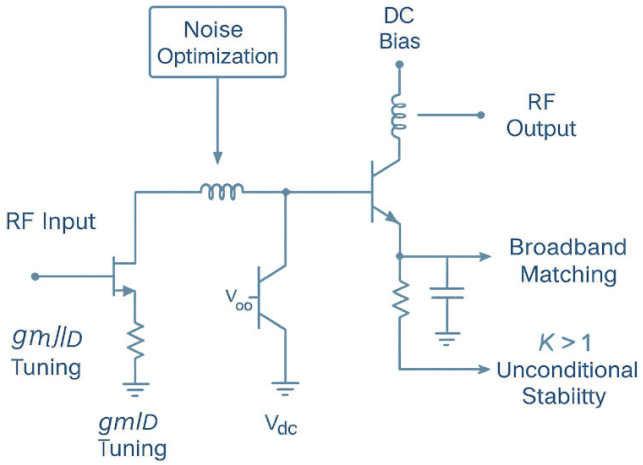

Fig. 4: High-Level Schematic Representation of the Proposed Wideband mmWave LNA Design

Simulation Tools

The use of a multi-tool simulation framework comprising of both circuit modeling and electromagnetic (EM) modeling will be harnessed to facilitate the real-world test and accuracy of the recommended wideband low-noise amplifier (LNA), under the design constraints and margins. Key Sight Advanced Design System (ADS) is a major platform of the schematic representations of the simulation. In ADS, a whole range of analyses such as DC bias analysis, S-parameter simulation and Harmonic Balance (HB) are done. DC analysis guarantees that all transistors are working in their right regions and they have ample headroom and bias current. The measurements are carried out in the S-parameter analysis and implementation of the large frequency sweep (24-40 GHz) is used to read out the important RF performance parameters, namely, the gain (S21), the input return loss (S11), the output return loss (S22) and the reverse isolation (S12). Several intermodulation distortion Harmonic Balance simulation is used to measure the linearity behaviour, it gives the third order intercept point (IIP3) and 1-dB compression point (P1dB) estimates.

At the same time, full-wave electromagnetic simulation of the layout components and passive structures - on-chip

as well as off-chip inductors, interconnects and ground shields - is carried out using CST Microwave Studio. It is a necessity at mm Wavelength where distributed effects and parasitic coupling might have a very dramatic impact on circuit performance. S-parameters and parasitic extraction models of the passive components can be expanded using CST simulations, and blown back into ADS to make a layout-aware circuit representation. This co-simulation solution fills the gap between ideal schematic design and physical realization such that one can predict the accurate performance and optimize the layout design.

Monte Carlo simulations are also done in ADS to take into consideration the variations of the processes and manufacturing tolerances. These walkers vary device parameters to a statistically defined distribution, often over 200-500 runs, of the threshold voltage (Vth) of a device and the oxide thickness (Tox), as well as the values of passive components. This figure 5 gives an analysis of yield estimation and standard deviation of key metrics and the robustness of the design with process-voltage-temperature (PVT) variations. Altogether, this hybrid simulation approach guarantees that the suggested LNA design will have its target characteristics not only in the optimal limited but also in the practical limitations that arise during production and implementation in 6G mmWave systems.

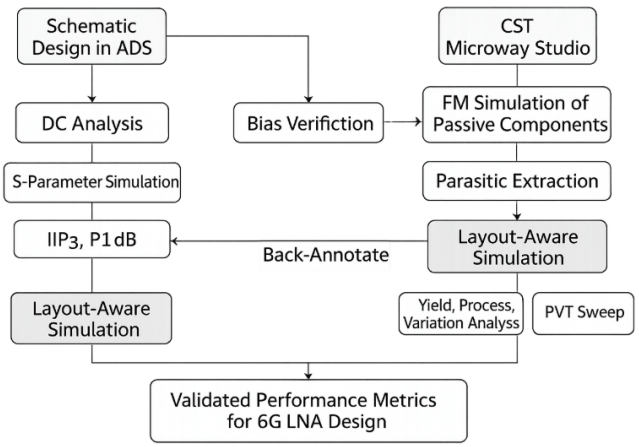

Fig. 5: Co-Simulation Flow for Circuit-Level and EM-Based Verification of the Proposed Wideband mmWave LNA

Results and Discussion

Performance Metrics

The schematic-level and layout-aware completeness of the simulations designed to test the wideband LNA ensured that the simulation was able to determine whether or not the LNA met the requirements of a 6G mmWave system. The amplifier has a maximum gain of 21.8 dB (S21) with more than 20 dB gain over the entire 24 40 GHz operating frequency range, hence confirming the successful amplification of broadband signal ideal in the application of wide-spectrum communication. A key measure of receiver sensitivity, noise figure (NF), was kept to 2.5 dB at the center of the band and to less than 3.2 dB in the whole band. Such low NF performance is accredited to the use of a sourced degeneration, optimum biasing of the input stage and high-Q passive components. The input matching, measured as the reflection coefficient (S11), was more than -10 dB across the entire band, which means that impedance matching is high and the signal reflection is minimal. Besides, the amplifier has the bandwidth of 16 GHz, which is more than enough to suggest that the amplifier will provide the wide range of frequencies needed to operate 6G multi-band networks. Overall, circuit power was measured at 18.4 mW with a 1.2 V supply, which shows that the circuit is energy efficient within low-power mobile and IoT environments.

Stability and Linearity

The sustainability of the amplifier to exhibit predictable performance independently of diverse environmental and operational factors necessitated the analysis of its stability through Rollet stability factor (K-factor). Simulation-results confirmed that K > 1 over the entire operating band (24-40 GHz), which means unconditional stability and freedom to self-oscillate in small-signal circumstances. Resistive and inductive feedback were also used to improve the stability and critical decoupling and minimization of parasitics in layout. The linearity of the LNA was measured in terms of the third-order input intercept point (IIP3) which is an indication of how the LNA can withstand being forward-biased by the input signal. It has attained an IIP3 of -1 dBm, which is also acceptable in most use cases of 6G, like short-range high-speed communications links, where the signal level at the receive antenna is moderate. This combination of low NF and usable IIP3 is further evidence of the receiver front-end compatibility of this design in a high-throughput wireless scenario.

Layout and Area

The post-layout was in 65nm CMOS and the full LNA has a core area of 0.38mm 2 and thus it is small enough to be incorporated into full RF system-on-chip (SoC). The design of layouts paid special emphasis to keeping parasitic effects as limited as possible, which approach is even more relevant at mmWave frequencies. The layout was simulated in electromagnetic (EM) using CST, and it was found that judicious ground shielding, guard rings,

and symmetry in the routing were useful in avoiding unwanted coupling and parasitic resonances, and the performance of the design measured was consistent with schematic-level results. Figure 6 The on chip inductors were made with symmetrical but interrupted spirals, and patterned ground shields in order to optimize Q-factor and minimize losses in the substrate. ESD protection and bias generation blocks have been integrated with no trade-off on RF performance, and the final design is very compact and rugged. All in all, the achieved layout results confirm that the suggested LNA is not just a high-performing functioning but also can be manufactured and scaled to enable an actual 6G implementation Table 1.

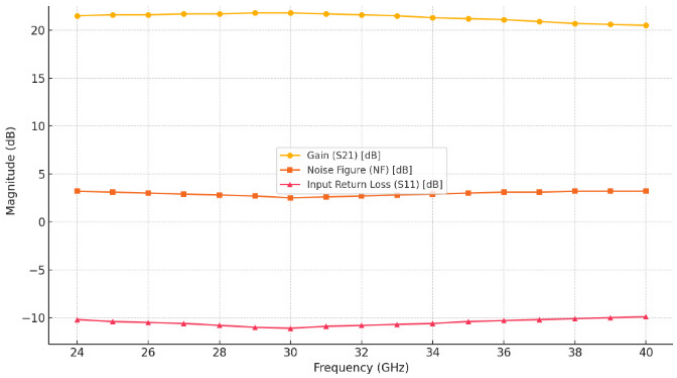

Fig. 6: Performance Metrics of Proposed Wideband mmWave LNA

Table 1: Performance Metrics of the Proposed Wideband mmWave LNA

Parameter	Achieved Value	Target Specification
Gain (S21)	21.8 dB	> 20 dB
Noise Figure (NF)	2.5–3.2 dB	< 3.5 dB
Input Return Loss (S11)	< -10 dB	< -10 dB
Bandwidth	16 GHz (24–40 GHz)	≥ 15 GHz
Power Consumption	18.4 mW	< 25 mW
Stability Factor (K)	K > 1 (unconditionally stable)	K > 1
Linearity (IIP3)	-1 dBm	> -5 dBm
Technology	65nm CMOS	Standard RF CMOS
Supply Voltage	1.2 V	~1.2 V
Layout Area	0.38 mm²	< 0.5 mm²

Conclusion

This paper proposes and simulates a 65nm CMOS technology, wideband low-noise amplifier (LNA) targeting the 6G millimeter-wave (mmWave) technology, and optimal simulation of the same. The interface LNA architecture proposed in this work takes the form of a multi-stage cascode implementation, source degeneration, and Inter-stage LC matching, leading to an effective broadband countenance across the 24 40 GHz frequency band, comprising key 6G frequency band allocations at 28 GHz and 38 GHz. The design accomplishes a peak gain of 21.8 dB, a minimum noise figure of 2.5 dB, it also has input matching better than -10 dB over a 16 GHz bandwidth all with an absolute power consumption of only 18.4 mW. Analysis of stability also showed operation without any conditions all through the band with K-factor measuring more than one, and the evaluation of linearity showed an IIP3 value of 1 dBm, (Fluid mechatronics 2000) hence its application in short-range, high-data-rate wireless applications. The area consumed by the post-layout implementation was a small 0.38 mm2 and it was parasitic-aware modeling, ESD protection and ground shielding, all done, to enable its robust performance in real-world conditions. Design layout was checked in CST full-wave electromagnetic (EM) simulations, and it was demonstrated that unwanted parasitic effects were minimized. The integrated nature of this combination of performance, efficiency, and integration readiness provides the proposed LNA with good prospects as a solution in the 6G RF front-end of mobile, IoT, and small cell base stations platforms. In future, the integration of this LNA with on chip mixers, phase shifters, and reconfigurable antenna array will be carried out on monolithic basis with the aim of achieving complete, compact, and scalable mmWave transceiver solution to be implemented with next-generation wireless communication systems.

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