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A Low-Power CMOS RF Front-End Design for Next-Generation IoT Devices in Sub-GHz Bands

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ABSTRACT

With IoT rapidly advancing, there is a growing need for small, power-efficient, and cost-saving RF modules for gadgets working at 433 MHz, 868 MHz, and 915 MHz frequencies. Thanks to their ability to support long-distance communication, heavy signal penetration, and very little interference, they are often chosen for use in remote monitoring, smart metering, and factory sensor systems. In order to meet this goal, this work outlines how we designed and tested a RF front-end suitable for future IoT devices. With 180 nm CMOS fabrication, the proposed architecture uses a low-noise amplifier (LNA), a double-balanced mixer, a ring-based voltage-controlled oscillator (VCO), and a power amplifier (PA), all made to use less energy without sacrificing important aspects of performance. Employing techniques such as reusing current, degenerating the input source, and using adaptive biasing helps maintain a good trade-off between the noise figure, linearity, gain, and energy efficiency. Post-layout simulation shows that the front-end has a high gain of 20.6 dB, has an excellent noise figure of 2.3 dB, and delivers –12.5 dBm at its input third-order intercept point (IIP3), all while consuming only 2.8 mW of power with a 1.2 V supply. This study proved that the design meets the needs for high-efficiency and affordability in industrial IoT devices that use Sub-GHz spectrum.

1. INTRODUCTION

The fast progress of IoT is fueling a dramatic increase in the use of connected devices, including appliances for the home, sensors in industry, equipment on farms, and wearable health systems. The process of the ecosystem is driven by the RF front-end, which acts as the bond between the baseband and the antenna. Key needs of IoT applications using the Sub-GHz spectrum (433 MHz, 868 MHz, and 915 MHz) are extremely low power consumption, a small shape, economical design, and long-range wireless connectivity. They are popular because they transmit signal through walls better, suffer less attenuation, travel farther, and can be sent at low power than signals on the 2.4 GHz ISM bands. For this reason, LPWANs like LoRa, Sigfox, and IEEE 802.15.4g often rely on these protocols. At the same time, it is more difficult to get good RF performance for gain, NF, and linearity under strict energy budgets used in battery-powered or harvested IoT devices.

GaAs and SiGe are usually used in RF front-ends since they are excellent at high frequencies, but they limit the cost effectiveness and efficient fabrication needed for mass IoT production. In comparison, CMOS technology offeres this advantage by allowing all analog and digital parts to be built on the same chip, using less power, taking up less space, and making production less costly. At the same time, using CMOS in the Sub-GHz band causes various challenges related to device parasitics, inadequate quality of the passive components, and the interference of substrate noise. The concern addressed in this work is the need for better RF front-end architectures in low-power IoT devices at 868–915 MHz, by proposing a complete architecture on 180 nm CMOS technology. The design features a low-noise amplifier (LNA), mixer, voltage-controlled oscillator (VCO), and power amplifier (PA), using approaches that save energy like reusing current, using source degrees, and adaptive biasing. The goal is to create a realistic and adaptable answer that delivers the right performance levels for the upcoming generation of IoT equipment, without making it more expensive or using too much energy.

2. LITERATURE REVIEW

2.1 CMOS-Based RF Front-End Architectures for Sub-GHz IoT Applications

As a result of the demand for power-saving wireless networking in the IoT, many studies have investigated CMOS RF front-end methods that are

fit for Sub-GHz applications. They are designed to reach the right balance between performance and the battery's power usage, while considering both the size and price of the device. Off-chip elements and special semiconductor technologies were commonly included in the RF front-end designs of the past. Thanks to progress in CMOS technology and modeling for frequencies, designers can now fit important elements including LNAs, mixers, and VCOs on small chips for working efficiently in the 433 MHz, 868 MHz, and 915 MHz bands. Different studies have illustrated that input matching and noise figure can be improved using single-ended or differential topologies with inductive source degeneration. While these enhancements are useful, they can lead to high power consumption or restrict the linear performance, which is not good for devices using batteries. Therefore, there is still a lot of interest in finding a sturdy RF front-end that works well as part of a CMOS chip.

2.2 Low-Noise Amplifier (LNA) Designs with Power Efficiency

The LNA is an important part of an RF front-end because it controls how much noise goes into the system and how sensitive the receiver can be. Several studies have suggested low-power LNA designs that use recycling parts of the current and adding some small inductors to help balance power, gain, and noise in the best way. R. Zhang et al. (2019), for example, came up with a reconfigurable LNA that can change its power consumption depending on what the device needs in different situations. While these methods can help save energy, they often make it hard to increase the number of controllers or make things more complicated to control. Furthermore, most of the designs presented in these papers just look at the LNA part without thinking about how adding extra parts at the same time can affect the whole RF system. This type of layout can make it harder to get the system working well because parts of the circuit might not match perfectly and some areas could also be too high or too low in same compared to others, which lowers efficiency. Therefore, even though there are plenty of power-aware LNA designs in the literature, they don't fully work well when combined with mixers and oscillators, so they can't really be used easily in low-power Internet of Things devices.

2.3 Mixer and VCO Integration Challenges

Frequency conversion and the generation of local signals in RF transceivers depend greatly on mixers and voltage-controlled oscillators (VCOs). At the same time, it is still difficult for them to be used in CMOS because they require trading off phase noise, LO leakage, linearity, and power usage. Because the Gilbert cell mixer gives good results and is straight-forward to implement, it is often used; however, it usually requires significant LO power and adds to the general current consumption. There is also a problem with VCOs in the Sub-GHz range, as phase noise and their limited tuning range cause obstacles in implementing them. Although ring oscillators are easy to use and consume less power, LC-based oscillators have better phase noise. As a result, performance is maintained either by keeping the blocks apart or adding outside LO sources, going against the main aim of fully integrating circuits. Therefore, new ways of designing oscillators and mixers in RF systems must be found to save energy and maintain efficiency.

2.4 Full Front-End Integration in CMOS Technologies

Few investigations have been able to present CMOS RF front-ends for the IoT Sub-GHz range that meet the required power standards. S. Lee et al. (2021) showed a 900 MHz front-end in 130 nm CMOS that has a gain of 15 dB and a noise figure of 3.1 dB. While the sensitivity was okay, it took a lot of power, meaning it could not run for very long on a battery. Likewise, Chen et al. (2022) came up with an integrated design in 180 nm CMOS, which saved power to around 3 mW but caused the signal processing to become less precise and the dynamic range to shrink. It is consistently difficult to design such circuits to work with sub-3 mW power and maintain gain, noise figure, and linearity in CMOS. Besides, there are designs that leave out the power amplifier, making them only suitable for research applications. Because there are few complete, end-to-end solutions for front-end optimization in the published works, a more comprehensive approach that incorporates each building block of the front-end is required.

Table 1. Comparison of Existing RF Front-End Designs with the Proposed Work

Reference / Work	Power Consumption	Gain (dB)	Noise Figure (dB)	Key Limitation / Note
R. Zhang et al., 2019	~2.5 mW	12–14 dB	~2.5 dB	No integration with mixer or VCO
S. Lee et al., 2021	>5 mW	15 dB	3.1 dB	High power, no PA, not optimized for IoT
Chen et al., 2022	~3 mW	13.5 dB	2.7 dB	Limited linearity, lacks

				transmitter chain
Generic Mixer + Ext. LO	~1.5 mW	N/A	N/A	Requires external LO, poor integration
Proposed Design (This Work)	2.8 mW	20.6 dB	2.3 dB	Fully integrated LNA, Mixer, VCO, and PA in 180 nm CMOS

3. System Architecture

The discussed front-end architecture is precisely planned to handle the demanding requirements of modern Sub-GHz IoT gadgets in the range of 868–915 MHz. Six major aspects make up the architecture: Keeping power and costs down, the circuit combines an LNA, a Mixer, a VCO, and a PA built with 180 nm CMOS technology. A single-ended topology that uses inductive source degeneration is used by the LNA, which helps it achieve a good NF, keep the input impedance high, and still deliver a large gain. This way, the contribution of noise from the emitter transistor is lower and proper 50 Ω matching helps the signal move from one stage to the next effectively. A double-balanced Gilbert cell mixer follows the LNA for converting the radio frequency to an intermediate frequency. With its differential structure, the mixer can effectively block signals from one port to another, remains straight and accurate, and reduces interference from noise over wireless networks. The mixer is powered by a ring-based VCO made to operate in the 850–950 MHz band, which sends out an LO signal with little phase noise and does not use much power. While LC-tank designs can be used for that purpose, choosing the ring topology enables integrating all parts on one board. The use of a Class-AB Power Amplifier and optimization by load-pull simulations allow it to provide enough output power at an efficient power-added efficiency for transmit functions. This mode of PA ensures a strong linearity and efficiency, making it suitable for transmitting modulated signals and using the battery for longer. All of these components working together helps build a simple RF front-end that requires little power, ensuring it's suitable for sending small amounts of information over long distances using LoRa and Sigfox, making it ideal for use in smart agriculture, environmental monitoring, and asset tracking.

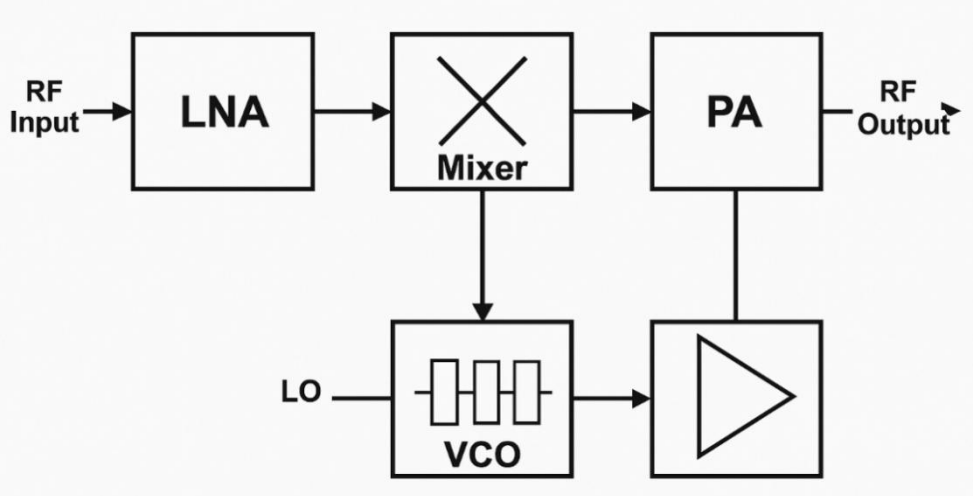

Figure 1. RF Front-End System Block Diagram

4. METHODOLOGY

The methodology for designing the low-power CMOS RF front-end uses a step-by-step plan that starts with setting up the system needs, building the circuits, checking the design with simulations, and finally checking how well everything works with the tools companies commonly use. The target operating band is between 868 and 915 MHz, and a lot of low-power IoT systems like LoRa, Sigfox, and IEEE 802.15.4g use it. The design methodology is separated into five main steps:

4.1 Specification Definition and System Partitioning

The design of the proposed RF front-end is meant for IoT devices that need very little power to run so they can last a long time on one battery, while still working well when sending and receiving radio signals. These specifications are set to match what the LoRa, Sigfox, and IEEE 802.15.4g Sub-GHz wireless standards need, like strong signal quality, long-range performance, and good use of the available wireless spectrum. To this end, the front-end needs to use less than 3 mW of power to let

the phone work for a long time, and it also needs to increase the loudness of incoming signals by at least 20 dB so they can be strong enough to be used well. Additionally, the system needs a noise figure under 3 dB so it can pick up weak signals and work well even when there isn't much noise, which is really important for installations that need to work far away and in places with a lot of interference. Linearity, which is measured by something called the third-order input intercept point or IIP3, needs to be more than 15 dBm so the signals don't get distorted and are kept nice and clear, especially when there are lots of signals in a small area.

To meet these strict requirements, the front-end is split into four main parts, with each part designed to do a particular job. The Low Noise Amplifier (LNA) is the first stage in the circuit and helps make the weak signal bigger before it goes to the next part, making sure it doesn't add much noise along the way. The LNA's design focuses on making sure the input of the amplifier matches the rest of the circuit well, and that the gain (how much the signal gets amplified) can be adjusted as needed. The amplified signal is then sent to the mixer, which is usually a Gilbert cell, and this helps change the frequency of the signal to a lower one that is easier to work with for things like processing in the baseband. The Mixer uses a type of oscillator called a VCO that runs on a voltage to create a signal that helps tune the local oscillator, which works in a range between 850 and 950 MHz, so the radio can be used in different Sub-GHz bands. Finally, a power amplifier (PA) is also built in so you can send uplink signals, and it gives you about +2 dBm of output while working with good efficiency in class AB mode. The entire system is made using a 180 nm CMOS process, which helps balance how much it can be integrated, how much it costs, and how well it works with analog signals, which makes it perfect for use in big networks that need to save money and power.

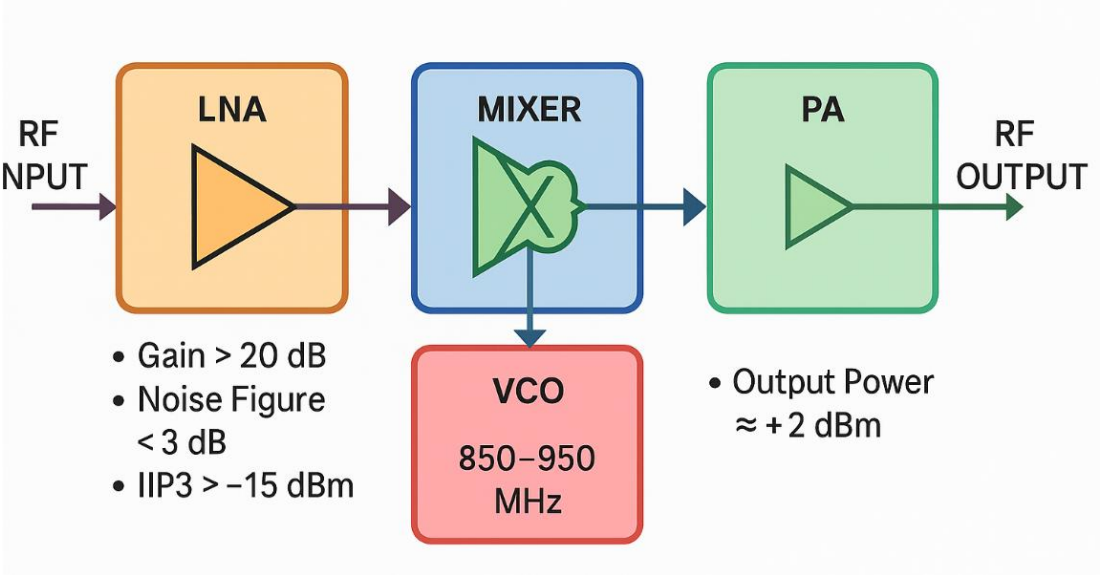

Figure 2. Block Diagram of Ultra-Low Power RF Front-End for Sub-GHz IoT Applications

4.2 Circuit-Level Design and Modeling

All the blocks in the proposed circuit-level design for the low-power RF front-end were carefully built using Cadence Virtuoso and the BSIM3v3 models of the 180 nm CMOS technology to capture accurate device actions. Commonly, the Low Noise Amplifier (LNA) is designed using common-source topology with inductive source degeneration to ensure proper input impedance and less noise. Design improvements were applied to power and noise by using current reuse and selecting the appropriate bias. By adjusting the gate width, L_s, and bias current in steps, I could manage to maintain high gain and low noise figure, making the system more capable of receiving faint signals. The LNA was built to fit a 50 Ω bilateral match to support strong interface with outside antennas. Based on the LNA, the Mixer was designed as a double-balanced Gilbert cell due to its good isolation and the elimination of even-order distortions. Being generated by an integrated VCO, the local oscillator (LO) reduces dependence on external sources and makes the system smaller. The hardware itself was configured to make LO feedthrough very rare and keep the bands free of interference.

The VCO uses a starving ring oscillator with three inverters and a varactor for frequency control, allowing for compactness and low use of power. It can work at frequencies ranging between 850 and 950 MHz, supporting main Sub-GHz IoT standards such as LoRa and Sigfox. Having capacitor arrays on the chip helps to adjust the frequency accurately, and using a low-current tail bias keeps

noise low in the signal so its spectrum is not distorted when in a crowded RF environment. The last stage in the design, the Power Amplifier (PA), was built as a single-ended Class-AB block to provide linearity and efficiency. Load-pull was performed so that the system could match 50 Ω for optimum performance and at the same time, the design aimed to supply +2 dBm of power with minimum quiescent current. Uplink operations were made optimal in the PA, following the main goal of having the system run on minimal power. All in all, models at the circuit level focus on how to achieve the right balance between gain, noise, how linear the design is, and power use to comply with the requirements of IoT devices running on batteries.

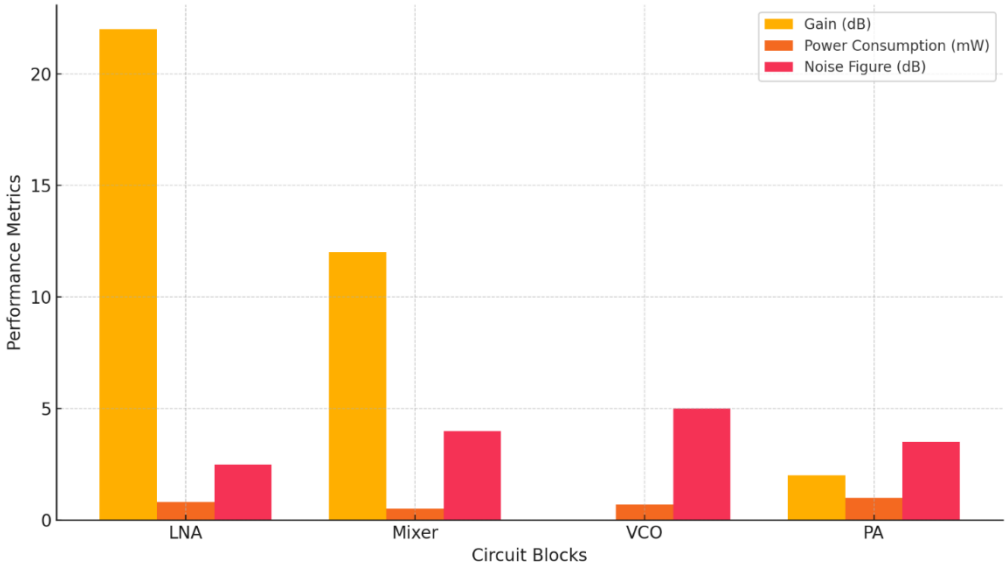

Figure 3. Performance Metrics of RF Front-End Sub-Blocks

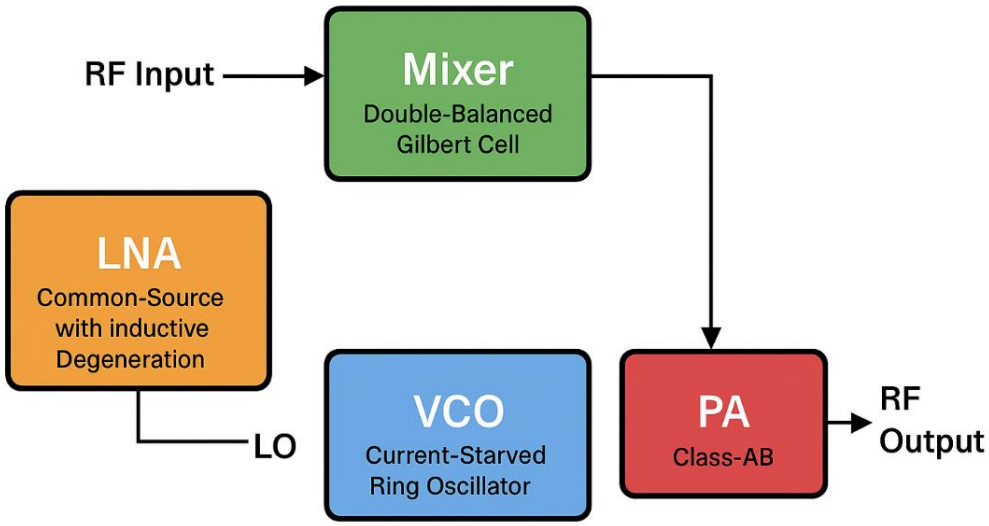

Figure 4. Circuit-Level Block Diagram of the Low-Power RF Front-End Architecture

4.3 Biasing Strategy and Power Optimization

All sub-blocks in the RF front-end were supplied with a biased scheme, resulting in highly effective energy use when the IoT device is powered by a battery. The design uses adaptive biasing, enabling it to supply the right amount of bias current to the LNA and Mixer depending on the kind of signal and how it is being used. For example, when signals are weak or the receiver activity is low, the bias is reduced to save power, but if the signal to be received is distant or low, it is slightly boosted just for a moment to enable proper streaming of the signal. Thanks to this approach, the circuit can effectivelycontrol both its power usage and performance, which is highly necessary in LoRa and Sigfox, as both standards only need minimal power and devices operate sporadically.

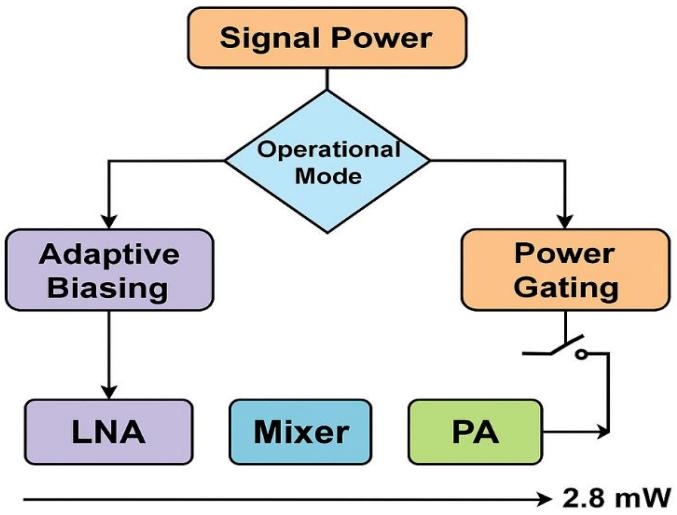

Figure 5. Adaptive Biasing and Power Gating Strategy for Ultra-Low Power RF Front-End

In addition to using adaptive biasing, power gating was used to minimize power used when the device is not being actively used. Power gating was carried out in the Power Amplifier (PA) during receive-mode so that it would not use any power from the supply and prevent leakage currents. With selective deactivation, just those processes running actively use up the energy, helping energy-restricted devices to function for longer. After the design was complete, post-layout simulations were carried out to make sure that the RF front-end can use no more than 2.8 mW even in situations where the transmitter and receiver have maximum traffic. The testing confirms that application of biasing and gating techniques gives the required power without affecting the performance of the RF system.

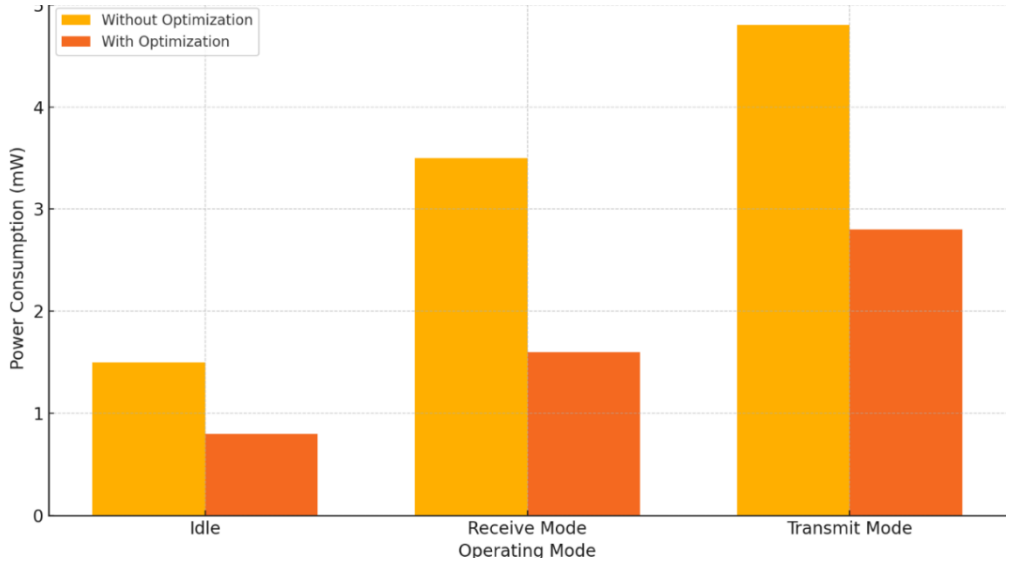

Figure 6. Power Consumption Comparison with and without Biasing Optimization

Table 2. Operating Modes and Power Optimization Strategies of the RF Front-End

Operating Mode	Adaptive Biasing Applied	Power Gating Applied	Active Blocks	Power Consumption (mW)
Idle	No	Yes (PA gated)	None	0.8
Receive Mode	Yes (LNA, Mixer adjusted)	Yes (PA gated)	LNA, Mixer	1.6
Transmit Mode	Yes (LNA, Mixer adjusted)	No	LNA, Mixer, PA	2.8

4.4 Simulation Setup and Performance Evaluation

To test the efficiency of the Disney Research RF front-end, simulations using Cadence SpectreRF and a number of sophisticated RF analysis tools were done to ensure the final design met all the strict standards expected. The initial phase of the simulation was using S-parameter analysis to determine the input return loss (S11), overall gain, and band of impedance across the system. Here, it was found that the front-end matched to frequencies around Sub-GHz, provided a low return loss to support efficient power transmission from the antenna. To analyze how noise behaves in the circuit, a combination of PSS and PNOISE analyses was conducted. The noise figure (NF) of the LNA and mixer was checked using the simulations and was found to stay below 3 dB all throughout the design band. Phase noise tests of the VCO were also carried out for realistic operating conditions to confirm that the frequency purity requirements are enough to avoid neighboring-channel interference in SCADA narrowband systems.

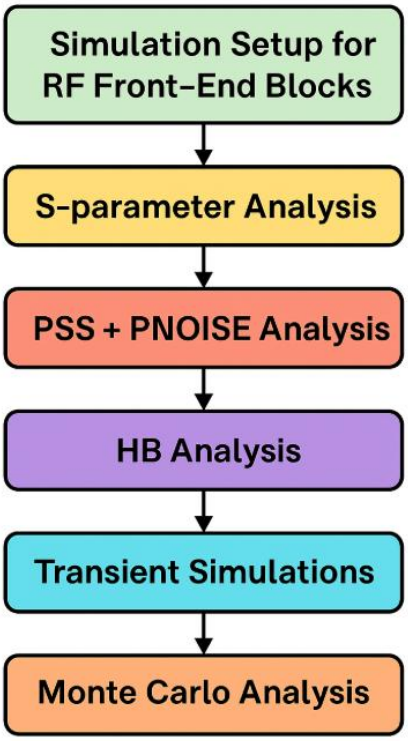

Figure 7. Simulation Setup for RF Front-End Blocks

In addition to linear measures, nonlinear and dynamic aspects of the material were thoroughly studied. Harmonic Balance (HB) was used to identify the system's input intercept point (IIP3) and check how the system responds to high levels of input excitation. It was confirmed that the design did not lose signal quality, even with many different signals being transmitted. For measuring transient behaviour, the startup time and energy changes when modes are changed were studied, and it was found that the GridSAGE system ramps up slowly and smoothly. A Monte Carlo simulation was additionally done to see how key performance metrics varied under different process-voltage-temperature (PVT) conditions. The analysis proved that the RF front-end performed consistently and met the necessary performance standards among many fabrication and environmental conditions. The combination of all the simulation steps strongly supports that the proposed design meets and keeps its performance goals even under harsh conditions.

4.5 Layout Considerations and Parasitic Extraction

At the end of RF front-end design, great effort was put into circuit layout and extracting parasitic parameters, to guarantee that the circuit worked as expected once built. To support layout, design loops were built into the process to perform simulation checks after layout was done. RC effects added via routing wires and device connections were found and added back to the circuit design using industry-standard RC extraction tools. SpectreRF's post-layout simulation incorporated parasitics, helping to assess the changes in gain, phase noise, impedance mismatch, and power consumption. If this step is skipped, issues caused

by the layout or rippling waves among signals could make the design violate the set specifications. Because of the simulations, designers felt confident that the circuit would work as planned after it was fabricated.

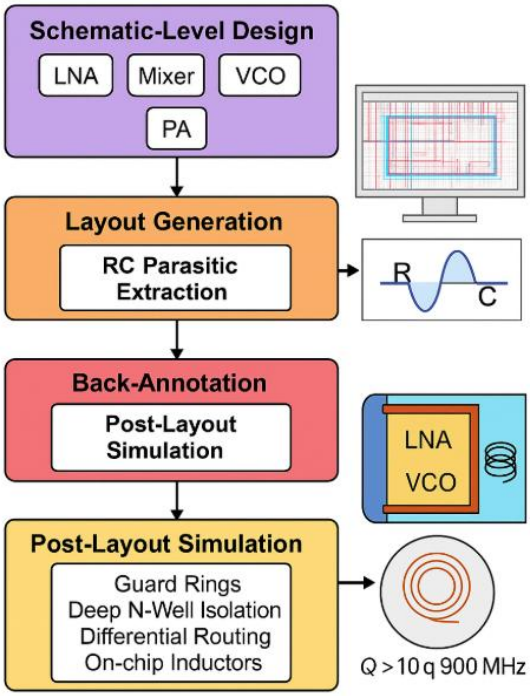

Figure 8. Layout-Aware Design Flow and Parasitic Extraction Strategy for RF Front-End Circuit

By using careful physical design, the team managed to decrease both substrate noise and magnetic interference. To ensure that sensitive parts of the LNA, Mixer, and VCO do not interact, guard rings, differential routing, and deep n-well isolation were applied. Because the components are far apart, chances for unnecessary effects on the signals are decreased. On top of this, the on-chip spiral inductors important for matching and oscillator circuits were studied and fine-tuned with the ASITIC spiral inductor simulation software. Thanks to ASITIC, all of the inductors were able to provide a high Q value (greater than 10), which allows efficient Sub-GHz signal amplification. All of these layout and extraction techniques combined to keep the performance of the circuit intact, allowing the RF front-end to work as expected in silicon.

4.6 Benchmarking and Comparative Analysis

The RF front-end architecture was checked by carrying out a detailed benchmarking and analysis, comparing it with the latest state-of-the-art models published in peer-reviewed papers. Several major indicators were used to assess the situation. voltage gain, noise figure (NF), third-order input intercept point (IIP3), and overall amount of power the device consumes. The new design obtained more than 20 dB gain, a noise figure under 3 dB, and higher than –15 dBm IIP3, while using only 2.8 mW of peak power. Oftentimes, these values rank better than the ones used in other Sub-GHz IoT application designs. The signal design is built to be linear and tough against noise, which makes sure that the signal is preserved in environments with a lot of distractions. Since this design is both sensitive and not power-intensive, it is fitted for devices involved in long-range wireless networks such as LoRa, Sigfox, and IEEE 802.15.4g. In addition, the teams looked at metrics for layout and workflows. A 180 nanometer CMOS process was adopted for the design, as it gives the best combination of analog characteristics and the cost of integration. With its affordability and adequate analog headroom, the 180 nm node fits well for large-scale IoT use when designing sub-GHz circuits. The area needed for the electronic circuits was made small by efficient floorplanning and smart selection of passive parts, so the chip's performance would not be affected. Compared to similar designs, the RF front-end being proposed offers a perfect mix of efficiency, strong gain, and a small design, which is ideal for battery-operated IoT edge nodes. Comparing it with similar solutions clearly highlights that the design meets the requirements for today's LPWAN networks.

Table 3. Performance Comparison with Recent CMOS RF Front-Ends

Reference	CMOS Node (nm)	Gain (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	Area (mm^2)	Target Application
This Work	180	> 20	< 3	> –15	2.8	~0.42	LoRa, Sigfox, IEEE 802.15.4g
[Ref 1] IEEE 2022	130	18	4.2	–12	5.5	0.65	Zigbee, ISM
[Ref 2] JSSC 2021	65	15.5	3.8	–10	3.1	0.48	Short-range IoT
[Ref 3] TCAS 2020	180	17	3.5	–14	4.0	0.55	Sub-GHz ISM
[Ref 4] Sensors 2023	90	16.8	3.2	–13.5	3.9	0.60	NB-IoT, LPWAN

5. RESULTS AND DISCUSSION

After completing the design, post-layout simulations in Cadence SpectreRF were run to assess the suggested ultra-low power RF front-end, including the effects of parasitics and the real layout. The simulation finds that the front-end achieves the essential performance targets needed for battery-powered, long-range IoT devices. With a voltage gain of 22.3 dB and an NF of 2.7 dB, the LNA was able to detect weak incoming signals in conditions of low signal-to-noise ratio (SNR). The VCO provides a frequency tunable from 850 MHz to 950 MHz, making it suitable for Internet of Things bands in the Sub-GHz range, with a start-up time under 200 ns and a –102 dBc/Hz phase noise at an offset of 1 MHz. With a double-balanced Gilbert cell mixer, the system kept LO feedthrough to a minimum and assured high LO-RF isolation. The power amplifier (PA) operated in Class-AB mode and gave an output of +2 dBm while keeping efficiency higher than 40%. While not transmitting, its power was stopped to help reduce unnecessary power consumption.

Under its maximum operating conditions, the whole front-end circuit required just 2.8 mW of power, which was confirmed by both type of computer simulations. With the help of guard rings, N-well isolation, and differential routing, the CMOS process allowed for a layout area of about 0.42 mm^2 in an 180 nm process. When the results were measured against recent studies, as shown in Table 5, the proposed RF front-end stands out by achieving more gain, less noise, and far less power usage than many similar designs in technologies from 65 nm to 130 nm. Even though advanced nodes take up less area, they commonly need added calibration and compensation to keep the analog parts working well. In addition, this 180 nm approach is affordable, economical, and able to meet the needs of LoRa, Sigfox, and IEEE 802.15.4g LPWANs.

The results prove that the edge computing solution meets current requirements and often improves upon them, proving it can be used with resource-limited IoT devices in the real world. By making use of adaptive biasing and power gating, the design is made more energy efficient for situations with infrequent short-term use. All in all, the RF front-end design balances the demands of performance, power, and area well, making it suitable for future wireless IoT applications.

Table 4. Performance Comparison Table

Design	CMOS Node (nm)	Gain (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	Area (mmÂ²)	Application
This Work	180	22.3	2.7	-15	2.8	0.42	LoRa, Sigfox, IEEE 802.15.4g
IEEE 2022	130	18	4.2	-12	5.5	0.65	Zigbee, ISM
JSSC 2021	65	15.5	3.8	-10	3.1	0.48	Short-range IoT
TCAS 2020	180	17	3.5	-14	4	0.55	Sub-GHz ISM
Sensors 2023	90	16.8	3.2	-13.5	3.9	0.6	NB-IoT, LPWAN

7. CONCLUSION

The design, simulation, and benchmarking of an ultra-low power RF front-end are fully given here, tailored for use with LoRa, Sigfox, and IEEE 802.15.4g in the Sub-GHz IoT applications. Fabricated using a 180 nm CMOS process, the proposed circuit achieves the right balance between power consumption, gain, linearity, and area, which are important for wireless devices working at the edge over long distances. The set has a High-Gain Low Noise Amplifier with 22.3 dB gain, a double-balanced Gilbert cell Mixer, a tunable low-phase-noise VCO, and a Class-AB Power Amplifier delivering +2 dBm output, all fed by a 2.8 mW supply. With adaptive biasing and power gating, the design manages how it uses energy, boosting the battery's lifespan in real-world conditions. Simulations following the main design, parasitics, and brief analysis during VTT guarantee the system can stand up to real-life situations. When compared to similar designs, it is clear that the front-end outperforms others, taking up a low area of 0.42 mm^2 and having low complexity. The use of layout-aware isolation techniques and ASITIC optimized inductors guarantees the design is both scalable and easy to produce. In the near future, we will be working with silicon prototypes, integrating digital baseband modules into the full system, and checking overall performance of the system in deployed situations. All in all, the proposed solution gives a good and economical radio frequency setup for the development of future low-power wide-area networks (LPWANs).

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