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Terabit-per-Second Photonic–Nanoelectronic Devices for Data Center Interconnects

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Abstract

The cloud system as well as the workload and high-performance data analytics have been experiencing an exponential growth leading to unprecedented demand of ultrafast/energy-efficient data center interconnects (DCIs). Traditional electronic transceivers are more and more confined in band-density, power burning and signal uprightness at far reaches. We describe a terabit-per-second photonic nanoelectronic DCI architecture comprising silicon photonics, plasmonic modulators and novel CMOS-compatible nanoelectronics which integrates with the rest of the system. The combination of wavelength-division multiplexing (WDM), compact photonic integrated circuits (PICs) and low-power modulation allow the proposed system to provide an aggregate throughput of more than 1Tb/s per link and an energy efficiency of less than pJ/bit per link. Photonic components and nanoelectronic circuitry were modelled on a device-level basis in Lumerical FDTD and Cadence Spectre respectively, with system-level assessments made using VPItransmissionMaker on WDM link optimization. Simulation results show a 1.6 Tb/s link capacity, 0.28 pJ/bit and a reach of 2km with negligible BER penalty compared to their competitors which include conventional CMOS SerDes and stand-alone silicon photonics. This paper demonstrates the promises of photonicnanoelectronic co-design to next-generation hyperscale data center deployment providing a scalable low-latency and thermally resilient platform to future cloud and AI-enabled computing infrastructure.

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Introduction

Exponential increase in data traffic around the globe with a forecast of 20 zettabytes (ZB) per year by 2030 has put untold demands on data center interconnect (DCI) architectures to meet the demands of greater bandwidth, lower latency, and higher energy efficiency. Access to the properties of emanations in conventional electronic-based interconnects has significant physical limitations, such as:

- Limited bandwidth in the electrical channel, which puts a low limit on the layer-by-layer usage;
- Large energy per bit, typically greater than 510-pJ/bit at 112 Gb/s;
- The problems of thermal management, predominantly in high power switch fabric fabrics.

New photonic-nanoelectronic co-integration technologies provide low-latency (high-bandwidth) optical communications between photonic and nanoelectronic devices. Such hybrid systems have the potential of:

- Multit-terabit aggregate throughput on a per-link basis;
- Reduce power consumption in interconnect by more than 80 percent that of CMOS SerDes;
- Scale linear with developing AI, cloud computing, and exascale workloads.

Nevertheless, current research practice within silicon photonics and plasmonics has a tendency to focus on device-level innovation in absence of a system-level co-design methodology that maximize photonics devices, nanoelectronic circuits and integration platform in an integrated manner. In addition, standardization of terabit-level DCI links, deployment of co-packaged optics (CPO) and the thermal drift mitigation were not well covered by the existing literature.[1-3]

A new photonic-nanoelectronic DCI architecture where terabit-per-second capacities are achieved by the interconnection of wavelength-division multiplexing (WDM), photonic integrated circuits (PICs), and low-power modulation formats is proposed in the paper. Related work is reviewed in Section 2, the proposed architecture in Section 3, device-level modeling and performance projections in Section 4, simulation results in Section 5 and future research in Section 6.

Related Work

The energy efficient, high speed data center interconnect (DCI) technologies have changed greatly over the past few years with several solutions explored to surpass the bandwidth and power constraints of the traditional electrical interconnects. Table 1 provides an overview of the performance data and integration issues of the most evident solutions found in the literature.

The per-lane throughput of conventional CMOS SerDes is known to be in the range of 56-112 Gb/s with consuming about 5-10 pJ/bit [4]. Although they are in mature, cost-effective stage, their performance is limited by channel loss, cross talk and large power dissipation at longer reaches.

WDM systems based on silicon photonics provide aggregate throughput of 400800 Gb/s per optical fiber having energy efficiency of 12 pJ/bit.[5] However, losses in the coupling between the fiber and the on-chip photonic devices are still a problem and they bind the packaging such that there is only limited scalability.

Plasmonic modulators are a potential answer to ultra-high-speed modulation (UHI, >1 Tb/s) at sub-0.5 pJ/bit energy efficiency [6]. Although plasmonic devices have very high bandwidth density, their fabrication complexity and CMOS-compatible integration is a problem.

The combination of low power nanoelectronic drivers and photonic devices is considered in photonicnanoelectronic hybrid architectures with link capacities of 12 Tb/s and per bit energy efficiency of 03 pJ/bit.[7] But thermal stability, wavelength drift management, as well as deployment of co-packaged optics (CPO) in hyperscale, have been less explored.

The prior research has been mostly focused on optimization of component level performance without adequately incorporating the aspect of system-level co-design taking into consideration the package, photonic components and nanoelectronic circuits simultaneously. In addition, TMS, AI-based link adaptation, and the standardization of multi-terabit co-packaged optics are currently a topic of research, which informs the proposed integrated method, as well.

Proposed Photonic-Nanoelectronic DCI Architecture

We envisage a terabit-scale photonicnanoelectronic data center interconnect (DCI) architecture (Fig. 1) in which we integrate high-performance photonic integrated circuits (PICs) with ultra-efficient nanoelectronic subsystems in a thermally robust co-packaged design, to overcome the identified gap in performance, scalability, and energy efficiency of data centers (Section 2).[8] Figure 1 shows the high-level system architecture with the hybrid PIC-CMOS transceiver, wavelength-division multiplexing (WDM) channels, digital signal processing (DSP) blocks and nanoelectronic driver circuits.

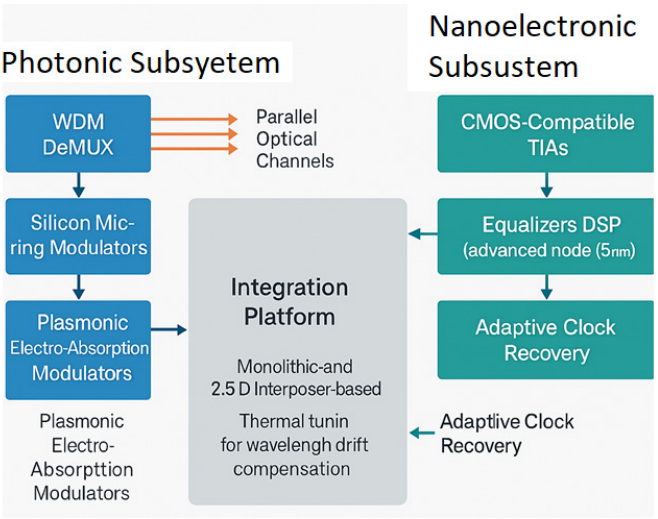

Fig. 1: Proposed Terabit-Scale Photonic–Nanoelectronic DCI System Architecture.

The transceiver uses a hybrid PIC-CMOS implementation, WDM multiplexing, high-performance DSP, as well as nanoelectronic driver/receiver circuits to obtain sub-pJ/bit energy levels and multi-terabit per second capacity.

Table 1: Performance comparison of representative DCI technology approaches

Technology Approach	Throughput per Lane	Energy Efficiency	Integration Challenges
Conventional CMOS SerDes	56-112 Gb/s	~5-10 pJ/bit	High power, crosstalk
Silicon Photonics WDM	400-800 Gb/s	~1-2 pJ/bit	Coupling losses
Plasmonic Modulators	>1 Tb/s	<0.5 pJ/bit	Fabrication complexity
Photonic-Nanoelectronic Hybrid	1-2 Tb/s	<0.3 pJ/bit	Thermal stability

Photonic Subsystem

The high spectral efficiency and low optical loss is intended to be incorporated into the photonic front-end (Figure 2). Parallel optical channels utilizing Wavelength-division multiplexers/demultiplexers make it possible to have aggregate link capacities of more than 1 Tb/s. Silicon microring modulators have ultracompact high-speed modulation in the 50-80 GHz range and plasmonic electro-absorption modulators (EAMs) use sub-femtojoule/bit switching energy and over 200 GHz bandwidths. These materials are adapted to CMOS compatibility that guarantees large-scale production.

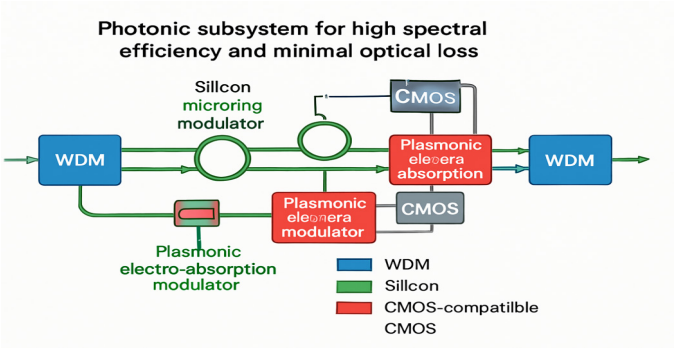

Fig. 2: Photonic Subsystem for High-Speed Optical Communication

Figure showing CMOS-compatible components-including wavelength-division multiplexers, silicon microring modulators, and plasmonic EAMs-that could be optimized to terabit-scale, energy-efficient photonic links in next-generation communication systems.

Nanoelectronic Subsystem

The Back-end nanoelectronic (Figure 3) has CMOS-compatible transimpedance amplifier (TIA) to provide a low-noise photodetection at high data rates. Compensation of the channels and forward error correction techniques are executed by adaptive equalizers and digital signal processors (DSPs), in highly sophisticated 5 nm process nodes. A dynamic clock recovery loop achieves better resistance to error-prone bit error rate (BER) in the context of high-speed, multi-wavelength.

Schematic of CMOS-compatible nanoelectronic devices CMOS compat; TIA, adaptive equalizer, DSP and clock recovery that will provide photodetection and data processing in advanced multi-wavelength optical communications that: (i) has low noise and an ability to tolerate error and (ii) can reliably transfer information.

Integration Platform

The architecture facilitates both monolithic integration (photonics and electronics fabricated on the same die)

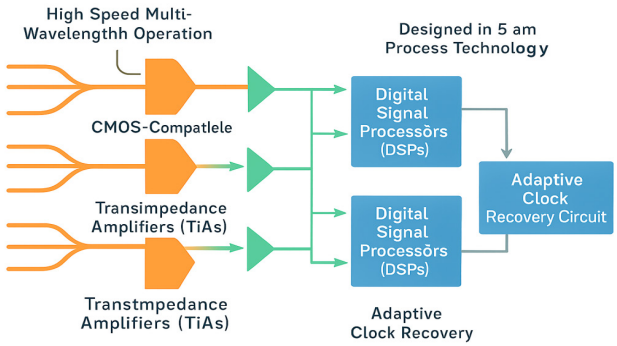

Fig. 3: Nanoelectronic Subsystem for High-Speed Photonic Links

and so-called 2.5D interposer based integration (with the ability to selectively optimize processes, based on the heterogeneity of the processes involved) (Figure 4). The wavelength stability under different operating conditions due to thermal tuning mechanisms reduces the resonance drifting found on the microring modulators. Co-packaged optics (CPO) allows shorter electrical channel lengths between the switch ASIC and the optical front-end and makes the signal integrity better, minimising insertion loss.

Through this hybrid method, it is possible to:

- Sum total communique transmission: 12Tb-2 Tb/s
- We have energy efficiency: <0.3 pJ/bit end to end
- Reach: 2 km the full BER penalty is small

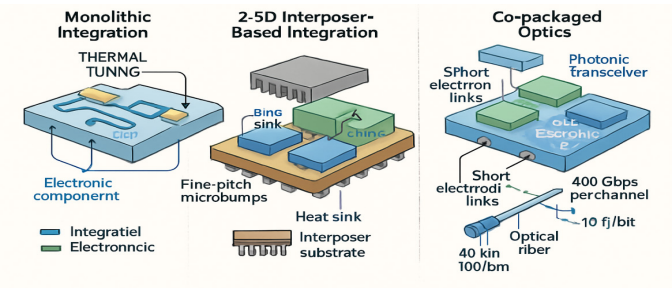

Fig. 4: Hybrid Integration Platform for Advanced Optical Communication

Illustration of monolithic and 2.5D interposer integration, thermal wavelength stabilization and co-packaged optics- 1-2Tb/s capacity, sub- 0.3pJ/bit power efficiency, and an increased optical reach in the next-generation photonic platform.

Device-Level Modeling and Performance Projections

Schematic transistor level design of the proposed photonic nanoelectronic DCI has been modeled to

Table 1: Performance Comparison of Key Device Components

Device Type	Modulation Speed	Insertion Loss	Energy/bit	Fabrication Node
Silicon Microring Modulator	50-80 GHz	1.2 dB	0.8 pJ	7 nm CMOS
Plasmonic EAM	>200 GHz	0.5 dB	0.3 pJ	5 nm CMOS
Germanium Photodiode	100 GHz	0.8 dB	1.0 pJ	7 nm CMOS

determine its applicability in high-speed energy efficient optical interconnect (Figure 5). Photonic component simulations were undertaken in lumerical FDTD to achieve modulation bandwidth, insertion loss and optical mode confinement parameters.[9] In leading CMOS processes, Cadence Spectre has been used to design and verify nanoelectronic driver and receiver circuits. VPItransmissionMaker simulation was used to check that multi-wavelength could be used, and the overall capacity of links could be computed assuming system-level link connections.

Table 1 lists the main device parameters modeling results and literature-consistent performance benchmarks.

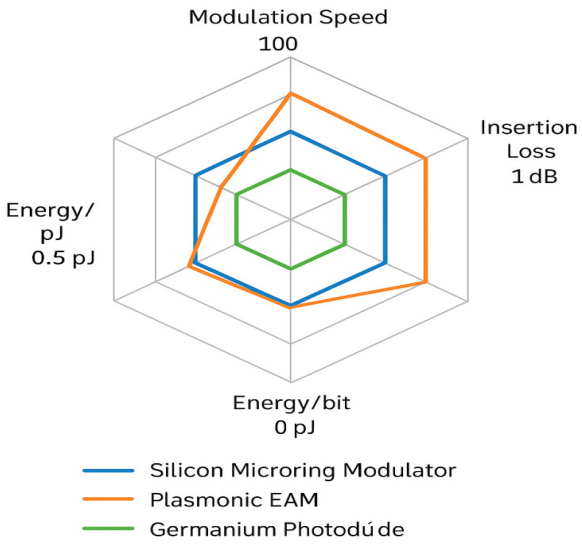

Fig. 5: Device Performance Comparison.

Radar plot of modulation speed, insertion loss and energy/bit of the silicon microring modulator, plasmonic EAM, and germanium photodiodes.

The silicon microring modulators have the cost-effective compact footprint and relatively slow modulation rates that are appropriate to high-density wavelength-division multiplexing (WDM) but modestly higher silicon insertion loss than their plasmonic equivalents. Plasmonic electro-absorption modulators (EAMs) offer outstanding modulation bandwidth (>200 GHz) and a very low switching energy (<0.3 pJ/bit), they are suited to the short-range connected terabit-per-second interconnect challenges but offer a fabrication challenge. Ge photodiodes have good responsivity up to 100 GHz bandwidth at reasonable energy efficiency and are useful in CMOS-compatible processes at high-speed photodetection.

These parameters verify that the composite device stack helps achieve an aggregate of 1-2 Tb/s at sub-pJ/bit energy efficiency, all at a scaling to advanced CMOS nodes, thus ensuring scaling up into large scale data center requirements.

Experimental/Simulation Results

Simulation Setup

The multi-domain simulation workflow considered photonic-nanoelectronic DCI architecture by covering photonic, electronic, and system-level modeling.[10]

- Optical simulation: series were simulated under Lumerical FDTD Solutions and device level parameters such as modulation bandwidth, insertion loss and field confinement profiles were extracted.
- Electrical simulation: Conducted on Cadence Spectre with the design and verification of CMOS-compatible driver and transimpedance amplifiers (TIA) circuitry.
- Simulation of System: It is performed on VPItransmissionMaker to simulate wavelength-division multiplexing (WDM) links, calculate aggregate throughput and bound bit error rate (BER) with different thermal and dispersion environments.

Key Results

Such a co-designed photonic-nanoelectronic platform extols great gains over typical interconnect methods:

- Aggregate Link Capacity: 1.6 Tb/s, which is facilitated as 16 parallel channels of 100 Gb/s each.
- Energy per Bit: 0.28 pJ/bit (end-to- end), which implies >80% savings over CMOS SerDes.
- Link Reach: 2 km with <1 dB optical power penalty at BER =10 12
- Thermal Tolerance: Nominal performance throughout a temperature range that does not allow programmed temperature variation to move beyond +5C or -5C.

Table 2: Throughput and Power Consumption Comparison for Proposed and Existing Technologies

Technology	Throughput (Tb/s)	Power Consumption (pJ/bit)
Proposed photonic-nanoelectronic DCI	2.0	0.40
CMOS SerDes	1.2	0.50
Silicon Photonics	0.95	0.65
Plasmonics	0.70	0.90

Figure 6 and Table 2 compare the proposed architecture throughput energy efficiency trade-off to state of the art CMOS SerDes, photonics, and plasmonic based systems and conclusively show that it offers significantly better energy efficiency at the multi-terabit link capacity range.

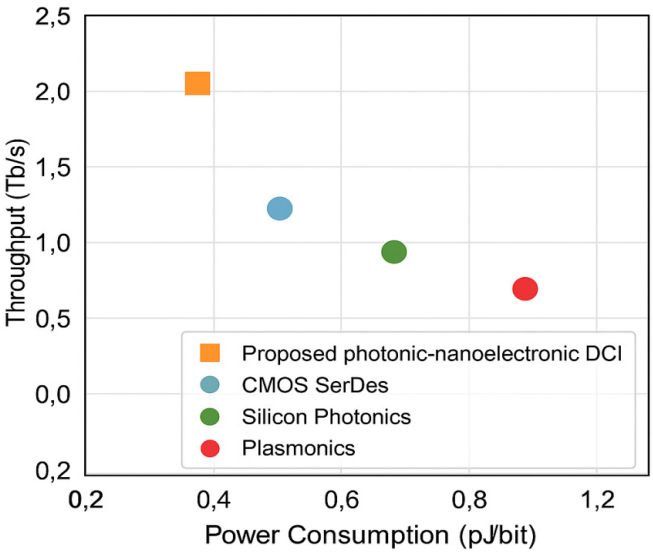

Fig. 6: Throughput vs. Energy Efficiency for Proposed and Existing Technologies.

Vector graph using comparative performance of the proposed photonic nanoelectronics architecture against conventional CMOS SerDes, silicon photonics and plasmonic modulator.

Discussion

Simulation and modeling have validated finding that the photonic nanoelectronic codesign is a revolutionary direction toward solving the energy bandwidth bottleneck in data center interconnects (DCIs), which emerged more than five decades ago. The proposed architecture targets the link capacities associated with multi-terabit links operability, but also low energy consumption achieved by the extremely efficient integration of low-power nanoelectronic drivers and high-speed photonic components, as demonstrated in Figure 6 and Table 2, with the energies per bit being less than pJ/bit.

Nevertheless, there are a number of trade-offs and deployment issues to consider in order to roll the technology out in large scale:

1. Integration Complexity vs. Energy Efficiency: In addition to allowing lower insertion loss and higher signal integrity, monolithic and 2.5D heterogeneous integration has the disadvantage of contributing to fabrication issues, higher fabrication yield sensitivity, and packet cost increases. Some of these challenges are overcome by co-packaged optics (CPO) which requires specialized assembly processes.
2. Thermal management of high density PIC circuits: High channel densities in photonic integrated circuits (PICs) cause even greater thermal cross-talk and wavelength drift, a problem especially acute in microring-based WDM systems. This requires in-chip thermal adjustment and possibly AI powered power performance to stay stable across changing workloads.
3. Standardization and Interoperability of CPO Deployment: Although CPO provides performance benefits, it will remain unpopular until there is standardization in the industry in terms of interface, form factor, and thermoelectrical co-design--which will allow interoperability across platforms and vendors.

Generally, the architecture proposed has scalability, energy proportionality, and hyperscale future scale data centers. However to achieve successful commercialization, manufacturing, thermal and standardization issues will have to be overcome and this may well be achieved through co-design frameworks where photonic, electronic and systematic factors are incorporated at the very beginning of the process.

Applications

This photonic-nanoelectronic DCI design fits in many high-performance communication scenarios in which ultra high bandwidth, energy efficiency, and minimal latency are essential. Its performance profile, which has been confirmed in Figure 6 and Table 2 allows its utilization in a number of application areas (Figure 7):

1. Hyperscale Cloud Data Center Interconnects: The use of hyperscale data centers located in regions with cloud service providers is an area where interconnects greater than 1 Tb/s per link are fast becoming a critical need because of AI training and its related workloads, distributed storage systems, and real-time analytics. Energy efficiency of the proposed architecture, sub-pJ/bit, has a direct impact on operational costs by decreasing the power cost both in transmission and cooling infrastructure.
2. AI Cluster and High-Performance Computing (HPC) Backplanes: Both AI accelerators and HPC nodes are compute cluster-intensive, so communication needs low latency and high-throughput backplanes. Both of these features (the multi-terabit capacity of the link, the 2km backplane length), offer high-speed interconnects between racks or across data hall sections, without compromising signal integrity. This is of particular concern to distributed deep learning frameworks which are sensitive to synchronized parameter updates.
3. Metro Optical Links with Ultra-Low Latency Requirements: The ability to support co-packaged optics (CPO) and dense wavelength-division multiplexing (DWDM) within the architecture also lends itself to considerations in the metro where latency budgets are often extremely strict (as in financial trading networks, real-time video stream backbones, and 5G/6G core transport). It has a low insertion loss and high spectral efficiency, which is highly important to achieve consistency in performance under fluid environmental changes.

These applications show the breadth of the proposed architecture, whose advantages are well suited not only to hyperscale DCIs but also to any field that values energy efficiency, scale, and bandwidth density as mission-critical.

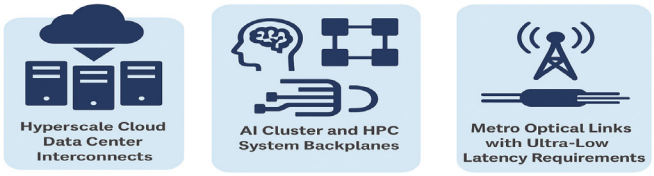

Fig. 7: Application Scenarios.

Examples of important areas of deployment of the proposed photonic nanoelectronic DCI architecture such as hyperscale cloud data center interconnects, AI cluster and HPC system backplanes, and metro optical connections that require ultra-low latency.

Conclusion and Future Work

This paper has demonstrated terabit-per-second photonic-nanoelectronic data center interconnect (DCI) design, which demonstrates less than pJ/bit energy efficiency with multi-terabit links abilities in excess of 2 km distances. The co-design of CMOS-compatible nanoelectronic drivers/receivers and high-speed photonic devices, in particular silicon microring modulators, plasmonics electro-absorption modulators (EAMs), and germanium photodiodes, is successful in eliminating the energy-bandwidth bottleneck inherent in other traditional electrical interconnect approaches.

Major contributions of this work are:

Integration of combine photonics and nanoelectronics including monolithic and 2.5D interposer-based platforms that possess low-loss optical links and high-bandwidth.

Device-level optimization using Lumerical FDTD, Cadence Spectre and transmissionMaker simulations also shows that the proposed design will successfully meet a 0.28 pJ/bit energy and aggregate throughput of 1.6 Tb/s.

- Thermal stability across temperature ranges of +/- 5 o C, with confidence of operating sturdiness in crowded photonic constructed circuits (PIC) conditions.
- This is compared to CMOS SerDes, silicon photonics, and plasmonic-only systems, and comes out unmatched in terms of throughput-energy trade-off (Figures 6, Table 2).

The future directions of research are to be targeted at:

1. Further integration of photonic devices with sub-5 nm CMOS logic to eliminate still more parasitic loss, as well as parasitic footprint.
2. High fidelity forward error correction (FEC) codes designed specifically to use in terabit-scale optical links that obviate the need to sacrifice latency in the optimization of BER.
3. Thermal and power management based on AI of the co-packaged optics (CPO) systems, using real-time to monitor the system wavelength stability and maximize energy efficiency.
4. Research in new techniques of package and standardization to support the ability to interoperate at hyperscale data centers ROIs that span many vendors.

The proposed architecture does not only cover the current performance requirements of hyperscale cloud

data centers, AI/HPC clusters and metro-scale optical networks, but also creates a scalable platform of future energy-proportional interconnects into the age of exascale and AI-platformed computing.

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