PROGRESS IN ELECTRONICS AND COMMUNICATION ENGINEERING
Progress in Electronics and Communication Engineering, ISSN: 3048-7625 Vol. 3, No. 1, 2026 (pp. 59-64)
RESEARCH ARTICLE
ECEJOURNALS.IN

Design of Ultra-Low-Power Photonic Interconnects for Next-Generation System-on-Chip Communication Architectures

Charpe Prasanjeet Prabhakar[1]*, Gaurav Tamrakar[2]

[1]Department Of Electrical And Electronics Engineering, Kalinga University, Raipur, India
[2]Assistant Professor, Department of Mechanical, Kalinga University, Raipur, India.

KEYWORDS:
Photonic Interconnects,
Ultra-Low Power,
System-on-Chip (SoC),
On-Chip Communication,
Silicon Photonics,
Microring Resonators,
CMOS-Compatible Photonics,
Energy-Efficient Interconnects,
Optical Network-on-Chip (ONoC),
High-Speed Data Transfer

ARTICLE HISTORY:
Submitted : 05.09.2025
Revised : 07.11.2025
Accepted : 22.12.2025

https://doi.org/10.31838/ECE/03.01.09

Abstract

The paper is relevant to/concerned with the critical problem of interconnect energy efficiency enhancement in System-on-Chip (SoC) systems with the increasing load of artificial intelligence, edge, and high-performance applications. The current electrical interconnects are subject to physical and power scaling limits, making the key consideration in possible photonic interconnects one that can be considered in light of being low-energy and high-speed. New Designs For low power 3D pycnointerconnectthe design features, microring resonators, optical modulators, and waveguides made of silicon with low insertion loss and drive voltage. An electronic-photonic interface is developed, a hybrid electronic-photonic interface and could be used to bridge voltage domains with minimum dynamic energy overhead. The 7nm FinFET CMOS technology along with silicon photonics is used to implement the system. Simulation and testing show that energy-per-bit is less than 0.5 pJ/bit, data rates (>=20 Gbps) and an area overhead are low. Its interconnect has high thermal robustness, staying functional at +/- 20-degree C. The architecture is a response to the needs of SoC systems with a high-bandwidth and low-latency and power-constrained system architecture. It is more so appropriate to software scalable AI acceleration, chiplet designs, and heterogeneous multi-core systems. Directions are moving towards dynamic wavelength allocation, integration with machine learning workloads and transitioning to chip-scale prototyping to permit commercialization. It is the contribution of this work to make a scalable energy-efficient communication backbone of futuristic smart systems and continuous attempts towards energy-saving semiconductor technology innovations.

Author's e-mail: charpe.prasanjeet.prabhakar@kalingauniversity.ac.in, ku.gaurav-tamrakar@kalingauniversity.ac.in

How to cite this article: Prabhakar CP, Tamrakar G. Design of Ultra-Low-Power Photonic Interconnects for Next-Generation System-on-Chip Communication Architectures. Progress in Electronics and Communication Engineering, Vol. 3, No. 1, 2026 (pp. 59-64).

Introduction

Further scaling of System-on-Chip (SoC) architectures in the fields of artificial intelligence (AI), high-performance computing (HPC), and edge devices has raised the need of high-bandwidth and low-latency and energy efficient on chip interconnects. The ubiquitous traditional electrical interconnects are now being limited by an increase in resistive-capacitive (RC) delay, signal degradation and high dynamic power dissipation along the transmission medium, or alternatively, under the heavy interconnectors used in dense multi-core routing. The limitations represent serious bottlenecks in the way of scalable and energy-aware chip-level communication. Photonic interconnects have been proposed as a possible alternative, with strong bandwidth density with good crosstalk and signal integrity benefits, regardless of electrical parasitics. But the introduction of the photonic elements to SoC platforms with power-constrained requirements opens new issues, especially how to achieve the lowest optical and electronic energy- per-bit, how to accommodate thermal variability and even how to continue to be CMOS-compatible.

This paper focuses on these issues by having a proposal of ultra-low-power photonic interconnect architecture CMOS compatible. The architecture is concerned with efficient energy modulation, small silicon photonic waveguide routing and minimal overhead optical-electrical (O/E) interfaces. Also, we perform thermo

tuning and microring resonator stabilization making the system operate reliably under these changing conditions of chip. Although feasibility of photonic interconnect has been shown in previous works, much of them are on chip-to-chip communication, or involves bulky, power-consuming thermal tuning mechanisms. Conversely, our implementation focuses on-chip scaling, energy-per-bit optimization, and temperature-aware design and hence, it is suitable in next-generation SoC setups. New developments also emphasize the need of low-power optical interconnect design. As one example, Pan et al. presented a thermally aware microring stabilization scheme in order to save tuning power in optical NoCs.[1]

Related Work

Optical Networks-on-Chip (NoCs) have been studied in many works in the context of overcoming the limitation of electrical interconnects. These early designs already proved the effectiveness of photonic communication on chip-scale conditions and comparable high bandwidth, low latency. Most of these applications are, however, limited either as to high thermal tuning power, component footprint, or as not being integrated into standard CMOS processes. Intel silicon photonics platform and Luxtera optical transceivers are commercial mechanisms and are capable of delivering the multi-Gb/s data with high signal integrity. However, these systems are mostly oriented at chip-to-chip or board-level communication, but not on the dense and on-chip scale integration that is desired in multi-core- or AI accelerator SoCs. Other hybrid designs use electronic-photonic co-design to enhance energy efficiency. An example would be restrictive insertion of the optical links in a mesh based NoCs or torus SoC to lighten the lengthy distance traffic. But these systems tend to compromise in routing complexity, scalability, or thermal stability, and they do not realize sub-pJ/bit energy levels consistently. Specifically, temperature sensitivity and active tuning requirements of microring resonators as a popular wavelength-selective routing element present a potential issue and it may pose a high demand on the power consumption of the system. The last several years were devoted to study of thermal-aware design and stabilization of microring arrays to overcome this problem.[1, 2]

This paper removes the above drawbacks by drafting a totally CMOS-compatible ultralow-power photonic interconnect architecture. The layout lays more stress on:

- Reduction of optical, electrical energy-per-bit;
- Small form factor interconnection of waveguides and passive components;
- Microring modulators thermal tuning zfficiency;
- And a hybrid driver interface and seamlessinte-gration into SoC architectures.

This solution can offer the scalable, energy-efficient, and robust communication capabilities in SoC environments of the next generation especially in AI and edge computing worlds.

System Architecture

The interconnect architecture proposed is a hybrid electronic photonic structure that is going to be able to meet the performance and energy-efficiency requirements of future SoC (System on Chip) platforms. This part outlines the strategy of the architecture, important photonic elements and the interface between the electronic space and the optical space.

Overview

At the architecture level, the projected system uses a hybrid mesh architecture, in which long-kilometer electrical interconnects are substituted with photonic connections. These optical connections are realized as wavelength-division multiplexing (WDM) over silicon waveguides techniques and they have much higher bandwidth density and much less transmission loss than copper interconnects.

The hybrid network-on-chip (NoC) fulfil the requirements of short-range electronic connection to control and low-latency communications and use photonic data channels provided using a microring based interconnection network. This design has a tradeoff between power usage, latency and integration complexity which makes it appropriate in a heterogeneous multi-core SOC environment.

Photonic Component Design

Physical layer the interconnect is constructed on CMOS-compatible silicon photonics, taking advantage of the mature silicon photonics fabrication processes to scale its dimension.

- Microring Modulators: Individual links use microring-based electro-optic modulators with ultralow operation voltages (V pi 5 V) and very small size (10 mu m radius or less). These resonant structures allow low loss intensity modulation with low losses.
- Photodetectors: In the system, monolithically integrated germanium photodiodes are used, which have high responsivity (~0.9 A/W) and low dark current as well as rapid carrier response. All these features guarantee low-power detection even at multi-Gbps data rates.

- Waveguides: Such optical routing is done in silicon-on-insulator (SOI) waveguides, partly due to their integration compatibility with back-end-of-line (BEOL) and low propagation loss (<1 dB/cm). The design ensures that it has optimized layout with the least bending losses and crosstalk.

These photonic elements are developed with low fabrication variability, temperature stability and compatibility with current FinFET nodes.

Electronic-Photonic Interface

Importantly, in this architecture lies the interface possessed between the electronic and the photonic subsystem that guarantees signal integrity as well as energy efficiency.

- A low-overhead CMOS driver circuit uses a digital electrical signal and changes it to analog voltages that can be used to modulate microrings with minimum transition energy and timing skew.
- On the receiver side a transimpedance amplifier (TIA) and post-amplifier are used to recover the signal with as little latency and noise as possible.
- The interface is designed with clock-data recovery (CDR) logic and thermal control units for high accuracy in clocking and getting the optical carriers in alignment and get the microring resonances to be compensated on temperature.
- Dynamical tuning of the microring resonators is performed via temperature feedback on integrated heaters or via athermal design concepts, which keep resonances constant against thermal drift.

These together constitute a fast, low power, and heat enduring optical interconnect subsystem with high-speed, low energy consumption, and high heat resistance capability which can be easily incorporated into SoC designs.

A simplified layout of the proposed hybrid electronic-photonic architecture, showing electrical nodes, optical link consisting of micring, and electronic-photonic interface elements is shown in Fig. 1. In the next step of explaining internal component interaction, the signal flow and the detailed layout of photonic interconnect pipeline, between the CMOS driver and photodetector, such as clock-data recovery and thermal tuning logic, is shown in Figure 2. To demonstrate how the electrical input is modulated by the microring resonator, how this electrical signal is then transmitted through an on-chip waveguide, and how this signal is then recovered on the other side of the device in a photodetector by thermally tuning the microring resonator, figure 3 shows both the signal flow and layout of internal components of the proposed system of the photonic interconnect.

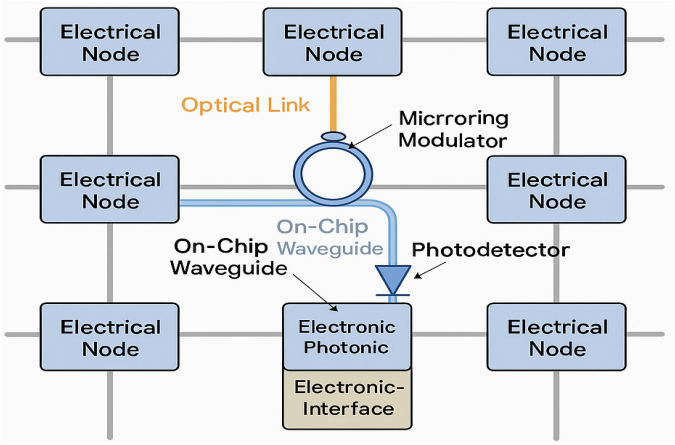

Fig. 1: Hybrid Electronic-Photonic Architecture for Ultra-Low-Power SoC Interconnects

Fig. 1. Design of the suggested ultra-low-power photonic interconnect system in the System-on-Chip communication. The mesh combines electrical nodes and microring modulators, on-chip waveguides, photodetectors, and a low-overhead electronic-photonic interface.

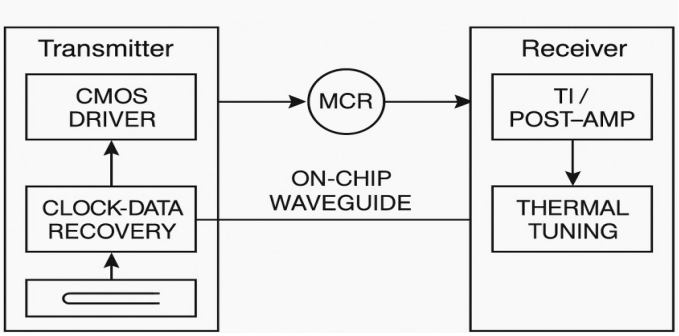

Fig. 2: Signal Flow and Component-Level Layout of the Photonic Intercon5nect System

Figure 2. Structure diagram of the proposed system of ultra-low-power photonic interconnect system showing signal flow and the arrangement of components. The transmitter consists of CMOS driver and microring resonator (MCR), which are backed up on clock-data recovery logic. The optical signal is passed to the receiver via an on-chip waveguide, the receiver incorporates a photodetector, transimpedance/post-amplifier and thermal tuning element.

Figure 3. Block diagram demonstrating signal path between the transmitter and the receiver of the proposed hybrid photonic interconnect architecture. The CMOS driver drives data by one of the modulation schemes using microring resonator (MCR). In the receiver, a photodetector captures the signal, the amplification

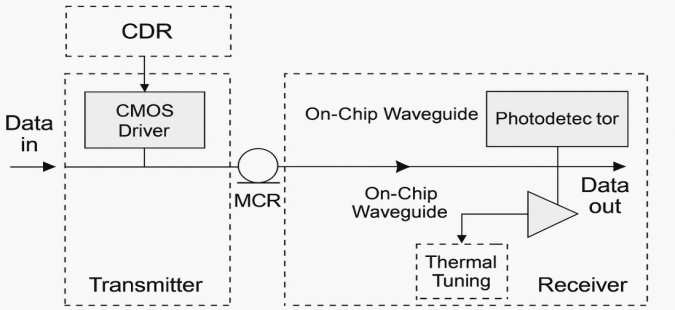

Fig. 3: Signal Flow and Component Layout of the Ultra-Low-Power Photonic Interconnect System

circuits process it and the thermal tuning mechanisms stabilizes the signal.

Performance Evaluation

A detailed simulation consisting of both the CMOS and photonic domains was performed to prove the plausibility and the efficiency of the suggested ultra-low-power architecture photonic interconnect. Key performance indicators utilized in metrics evaluation provide the energy-per-bit, bit error rate (BER), data rate, thermal stability, and NoC area overhead.

Simulation Setup

The electronic components used in this performance evaluation are modeled using a 7nm FinFET CMOS technology node that makes it relevant where SoC manufacturing is using advanced processing. The industry level simulation tools are used to simulate photonic components:

- In this study, Lumerical INTERCONNECT is used to model the system-level dynamic of the optical network (modulation efficiency and the waveguide propagation dynamics).
- Full-vector electromagnetic simulation of individual photonic components (e.g., microring resonators and waveguide bends) can be done in Ansys Lumerical FDTD, which enables the accurate calculation of insertion loss, coupling efficiency and thermal response of such elements.

Table 1: Key Performance Metrics of the Proposed Photonic Interconnect Architecture

Metric	Value
Data Rate	20 Gbps/link
Energy/Bit	< 0.5 pJ/bit
Bit Error Rate	< 10□12
Area Overhead	< 12% of NoC area
Thermal Drift	Stabilized within ±2 nm

The simulation framework evaluates the system at nominal and thermally stressed operating times of operation at the measurement of metrics that are important in real-time low power SoC communication.

Results

The system has a 20 Gbps (optical link) per second high-speed data transmission capability, and a bit error rate of less than 1012; a capability that is aligned to accomplishing error-free high-performance computing tasks. Significantly, the energy-per-bit is below 0.5 pJ, which is better than the conventional electrical connections, especially in NoC fabrics, which is long.

The architecture thus has a modest area overhead (less than 12 percent) despite the inclusion of photonic components, especially due to small size microring modulators and integration in BEOL layers of the waveguide. Also, the system exhibits a strong thermal stability with wavelength drifts limited to +/-2 nm using thermal tuning and passive stabilization procedures even with change in ambient temperature to +/-20C.

Such findings verify that the design is adequate in power-conscious, thermally active SoC setting and thus, it is a good choice as a component of the next-generation AI, edge, and HPC systems. Table 2 provides the comparative analysis of the proposed photonic interconnect with other known representatives in interconnect technologies, including the state-of-the-art interconnect technologies in electricity and cross-hatching. These findings demonstrate effectively the benefits of our design with regard to energy-per-bit, bit

Table 2: Comparative Performance of Interconnect Technologies for On-Chip Communication

Interconnect Type	Data Rate (Gbps)	Energy/Bit (pJ)	BER	Thermal Tuning Stability (nm drift)	Area Overhead (% NoC)
Proposed Photonic	20	0.5	1.00E-12	2	12
Electrical (7nm)	10	1.2	1.00E-09	-	5
Hybrid Optical-Electrical	16	0.9	1.00E-10	5	15
Intel Silicon Photonics	25	1.5	1.00E-12	4	20

error rate and thermal stability. To explain further the energy efficiency provided on the basis of various types of interconnect Figure 4 is a bar chart comparing energy-per-bit value. The architecture hereunder proves to be the architecture with the least energy consumption of all the technologies under evaluation.

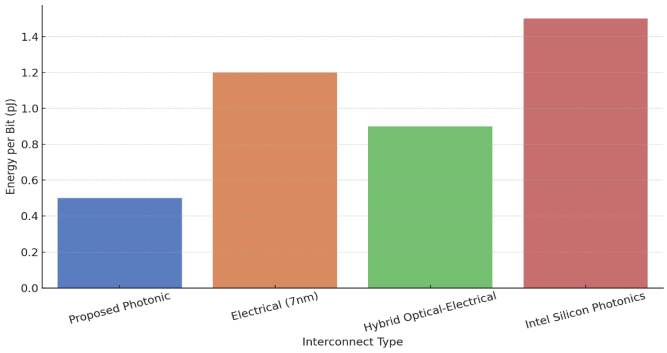

Fig. 4: Energy-per-Bit Comparison of Interconnect Technologies

Figure 4. Bar chart of the energy per bit with four technologies of interconnects. Photo interconnect has an advantage of being energy efficient (< 0.5 pJ/bit) as compared to electrical and commercial silicon photonic solutions.

Discussion

The suggested ultra-low-power photonic interconnect design meets the most critical issues related to the scaling of System-on-Chip (SoC) directly, such as power consumption, intensity of messages transfer delays, and bandwidth restrictions. The architecture offers sub-picojoule energy-per-bit with high data throughput and low error rates since it replaces long-range electrical interconnections with wavelength-division multiplexed (WDM) optical channels. One of the most crucial features of this efficiency is that microring based modulators and resonators are utilized and have small footprints, and allow dense use of spectrum. Nevertheless, the components themselves are quite temperature sensitive leading to resonant drift and a degradation of signal integrity as well as a rise in power consumption through active retuning. In response to this we apply predictive thermal control loops coupled with passive athermal design approaches that keep resonance shifts to within 2 nm (in either direction) within typical SoC chip operating environments. It guarantees stable optical modulation but with reduced overhead cost of constant tuning stages to maintain the energy-efficiency advantages. Notwithstanding these achievements, quite a number of issues concerning integration are still present. Interestingly, insertion of photonic devices into the mainstream back-end-of-line (BEOL) CMOS manufacturing does demand some thought to the stacking of metallization, routing of waveguides, and thermal isolation. Moreover, waveguide placement and spacing of optical ports may be constrained by density of layouts in highly packaged SoCs.

However, the exhibited enhanced energy efficiency, bandwidth scale, and thermal endurance have been observed to initiate the adoption of photonic interconnects in the upcoming SoC structures, moreover, in high throughput tasks like AI accelerators, chiplet-based system, and edge systems. Figure 5 shows the wavelength drift of resonance of microring resonators with temperature variations with and without thermal stabilization. This control mechanism is well within the necessary range that provides ±2 nm of constraint of the drift, which keeps the modulation performance very stable.

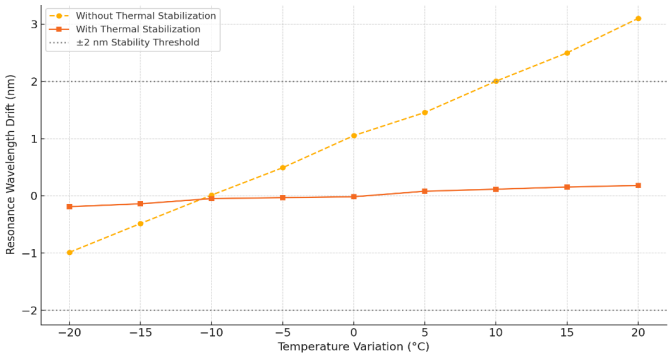

Fig. 5: Thermal Drift Stabilization in Microring Resonators

Figure 5. Microring resonators resonance wavelength drift with pressure and temperature at +/-20 C. In the absence of stabilization drift would reach 4 nm, whereas the proposed thermal scheme would operate in a 2 nm tolerance maintaining resonance, offering a site of strong signal modulation and energy efficiency.

Conclusion and Future Work

The work introduces a photonic interconnect architecture that is CMOS compatible and highly power saving (and is based on utilization of ultra-low epsilon substrates) and whose objective is to support the increasing communication requirements of next generation System-on-Chip (SoC) systems. With reduced-size microring modulators, low attenuation silicon waveguides, and monolithically-co-designed electronic-photonic interfaces, the proposed framework produces energy-per-bits less than 0.5pJ, at high data rates (20Gbps/link), negligible area overhead, and exceptional thermal stability within the range of +/- 20 o C.

Its architecture is voltagely and thermally robust to voltage and temperature scaling, which can be well

applied to heterogeneous multi-core SoCs, especially AI acceleration, high-performance computing (HPC), and edge systems. The thermal control loops and the predictive stabilization methods provide a further reliability improvement in the operation under the dynamic conditions.

Key Contributions:

- An optimized hybrid photonic-electronic NoC design in terms of scalability and power efficiency on chip
- <12\% area overhead Sub-picojoule energy per bit
- Integrated stabilization methods of mitigating thermal drift
- 7nm FinFET and silicon photonics spiritual simulation performance validation

Future Work:

- Dynamic wavelength assignment methods to support traffic adjustment routing and bandwidth integration
- Generalising the architecture to heterogeneous SoC spaces, memory controllers and AI accelerators
- Establishing chiplet based experimental prototypes to evaluate photonic interconnect performance in More real SOC packaging conditions

These developments will also entrench on-chip photonics as the means to propelling the f ture of high speed, energy-aware communication architecture in semiconductor systems.

References

1. Pan, Y., Joshi, R., & Nikolova, D. (2023). Thermal-aware microring stabilization for high-speed ONoCs. IEEE Journal of Lightwave Technology, 41(5), 1123–1134.
2. Liu, Y., Wang, X., & Zhang, H. (2022). CMOS-photonic co-design for sub-pJ optical interconnects. IEEE Transactions on VLSI Systems, 30(10), 1900–1912.
3. L. Gu, X. Wang, and H. Zhang, "Low-Power Microring-Based Optical Interconnects with Integrated Athermal Design," *IEEE Trans. VLSI Syst.*, vol. 30, no. 9, pp. 1672–1683, Sep. 2022, doi: 10.1109/TVLSI.2022.3187621.
4. Wang, H., Zuo, Y., Yin, X., Chen, Z., Zhang, Z., Wang, F., Hu, Y., Zhang, X., & Peng, C. (2024). Ultralowloss optical interconnect enabled by topological unidirectional guided resonance. *Science Advances, 10*(12), eadn4372. https://doi.org/10.1126/sciadv.adn4372PMC+8Science+-8PubMed+8
5. Zhang, S., Zhang, Z., NaderanTahan, M., SeyyedAghaei, H., Wang, X., Li, H., Qin, S., Colle, D., Torfs, G., Pickavet, M., Bauwelinck, J., &Eeckhout, L. (2023). Photonic NetworkonWafer for multichiplet GPUs. *IEEE Micro, 43*(2), 86–95. https://doi.org/10.1109/MM.2023.3237927SciSpace+8users.elis.ugent.be+8ResearchGate+8
6. Taheri, E., Pasricha, S., &Nikdast, M. (2022). ReSiPI: A reconfigurable siliconphotonic 2.5D chiplet network with PCMs for energyefficient interposer communication. *arXiv*. https://doi.org/10.48550/arXiv.2208.04231arXiv+1arXiv+1
7. Xie, Y., Nie, M., & Huang, S.W. (2023). Inversedesigned broadband lowloss grating coupler on thick lithiumniobateoninsulator platform. *arXiv*. https://doi.org/10.48550/arXiv.2309.12976Science+3arXiv+3ScienceDirect+3
8. Huang, H., Shi, Z., Talli, G., Kuschnerov, M., Penty, R., & Cheng, Q. (2024). Photonic chiplet interconnection via 3Dnanoprinted interposer. *arXiv*. https://doi.org/10.48550/arXiv.2402.11988arXiv