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Ultra-Low-Power VLSI-Enabled Embedded Systems for Neural Prosthetics: Toward Scalable and Real-Time Brain–Machine Interfaces

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Abstract

BMIs and neural prosthetics bring a world-revolutionizing promise in terms of defeating sensory and motor impairments in patients with neurological deficiencies. The current systems have severe drawbacks usually in the aspects of energy efficiency, effective interfacing with hardwares, and real-time capability, which renders them inappropriate in several wearable or implantable applications over a long period. The given paper suggests an ultra-low-power embedded architecture based on VLSI that has been especially tailored to overcome such limitations and facilitates elastic resource-constrained neural signal processing in real-time. The main aim of this study is to develop the compact, energy-efficient system-on-chip (SoC) platform which will consist of neural signal acquisition, spikes-based preprocessing, and embedded classification consumption of minimum power. The system is equipped with subthreshold analog front-end, hardware-efficient spike detectors, and a lightweight, embedded neural decoder combined with a dynamic power management unit, to reduce the energy requirements according to the demand of the workload. Simulation and FPGA-based prototype show that the system is capable of processing up to 64 channel of neural traffic at a rate exceeding 300 000 channels/second with average power-consumption below 120 micro-watts/ channel and a total processing-latency of 2.8 milliseconds. A comparative study shows major reduction in the amount of power consumption (~70%) compared to existing designs, without killing the signal fidelity or the decoder accuracy. This shows the functionality of the offered architecture and makes it appropriate to be implemented in next-gen neural prosthetic systems.In summary, the candidate VLSI-based embedded system offers a good way of creating ultra-low-power, real-time brain machine interfacing that can perhaps be used in an implantable biomedical device, adaptive neuro prosthesis, and closed loop neural control machine.

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Introduction

Brain-machine interfaces (BMIs) and neural prosthetics are an emerging field within neurotechnology research, promising new system capabilities such that loss of motor or sensory, and even higher-level cognitive, control can be restored in individuals with spinal cord injuries, neurodegenerative diseases, or limb amputation. These systems have the ability to pose a significant change on the type of life that affected persons will lead since they are designed to facilitate direct communication between the brain and the outside world. The key to the practicality of BMIs is to be able to learn neural signals in real time, in high fidelity and low latency. Nevertheless, there are major challenges in taking this technology out of the laboratory into a form that is practical and accessible in clinical use, both by the size of the equipment as well as its power consumption and ability to scale computationally.

The established BMI and neural prosthetic platforms usually utilize power-hungry digital signal processors

to conduct neural decoding and control operations, or exploit peripheral computing resources. Although these architectures can be very useful in controlled conditions, they cannot effectively be used in portable or implantable applications over a long period because of high power usage, thermal limitations and insufficient integration possibilities. In addition, the demands of multi-channel signal acquisition and real-time processing, at a high resolution, only worsen the energy and processing requirements. This makes this a basic conundrum; the way to build an embedded neural processing system that stays real-time, and scale without being reinvented, yet having the opposite extreme (power and area) constraints as biomedical applications.

The present paper proposes an exclusive architecture of ultra-low-power embedded with VLSI design principles that can solve this urgent gap. The recommended solution is to include analog front-end circuits, hardware efficient neural signal processing units, and power management approaches into a small system-on-chip (SoC), potentially reducing the energy consumption without breaching real-time responsiveness. The recent developments in subthreshold circuit design, data encoding based on event operation, and low-power embedded computing provide good support to such systems, and allow highly-optimized implementations to be made, applicable to closed-loop neural prosthetic systems.

This primary goal of the study will be to develop, build and test aML-cefficient scalable ultra-low power VLSI based embedded interface that can allow: real time neural signal acquisition, processing and classification. To be deemed suitable as a long-term solution in implantable or wearable medical devices, the system operates with minimal power consumption and has low latency and multi-channel capability. The study proves the possibility of achieving high-performance neural decoding at low energy cost on future, energy-limited embedded computing platforms at low energy cost through detailed system modeling, simulation and prototyping and signifies a significant step towards real life patient ready neural prosthetics systems.

Related Work

A rising field of research has been the development of the low-power embedded devices in the field of the neural prosthetic applications due to the growing need of the real-time brain-machine interfaces (BMIs) that are energy-efficient and shall have the scalability. Several research projects have striven to increase neural signal accessibility, spike localization, and on-chip type determination, under the work-based restrictions of wearable or implantable biomedical equipment.

Real-time processing of neural signals using FPGAs became very popular due to the ease of configurability and programmability. Another architecture was proposed by Zarei et al.[1] that used a combination of FPGAs and implantable interfaces and was fast enough to run in real-time, but very inefficient with regard to energy consumption and thus could not be used in long-term implants. Sharma et al.[2] reported a low power neural classification system on FPGA-SoC with machine learning accelerators in purpose, but the system still consumed more than 1.2 milliwatts per channel which is unacceptable in ultra-low-power biomedical systems.

There are a number of custom ASICs which are designed to minimize power. A renowned paper by Harrison and Charles[3] presented a CMOS amplifier that is more suitable in neural recording, but uses only 4 microWatts of power per channel. Although, it was a big step in the direction of energy efficient analog front ends it did not have embedded real-time capabilities. The 128-channel wireless interface introduced by Chae et al.[4] combined the extraction of spikes with the use of an ultra-wide-band transmitter, but spatial resolution and energy use compromises reduced general applicability. Chen et al.[5] went further to have classification embedded within the neural signal processor with the use of support vector machines (SVM) which allows closed-loop control. However, the power consumption was reported as greater than 1 mW/channel, which is rather difficult to use in long term wearable or implantable applications.

In addition to dedicated biomedical hardware, signal processing operations have been accelerated using reconfigurable computing to facilitate faster execution and more extensible machine learning capabilities in workflows.[6] These ideas show potential in developing neural prosthesis devices in the future where they will need to adapt to changing neural signals. Also, the current focus on wireless sensor networks and energy harvesting technology[7] supports the idea of sustainable means of energy in ultra-low-power electronics directly applicable in the use of embedded neural prosthetic platforms.

Denoising and classification of the biomedical signals have also been considered using the advanced signal processing techniques. Recently, preprocessing based on a wavelet was also used in combination with LSTM-CNN based deep learning models to process ECG signals that provide a future potential of a successful application of the hierarchical feature learning and time-specific feature learning in low-power health monitoring.[8] The architectures were not used with raw neural signals yet; nevertheless, they can guide the future embedded

classifiers on prosthetic devices. Also the new RF systems like reconfigurable antennas in cognitive radios[9] and eco-friendly material based electronics[10] is capturing our attention in recent times which bring adaptivity in hardware platforms and the importance of sustainable designs and this too is emerging in biomedical VLSI systems.

In brief, hopefully this research fills in the loophole of a fully integrated, ultra-low-power, and real-time embedded systems for neural prosthetics. It fills this gap by proposing a VLSI enabled architecture based on energy-efficient, scalable, and closed-loop in an effort that can help realize the practical use of BMI platforms in the future.

System Architecture

Overview

The proposed embedded system based on VLSI can operate in real-time, with infinitesimal amount of power, and sufficient power to handle neural signals, and is designed with potential implementation as peripheral members of a neural prosthetic system. The system is a conglomeration of five major components which include a neural front end amplifier array, spike detection, and feature extraction, a low power embedded processor complete with integrated classifier, wireless transmission interface, and dynamic power management controller. All the components are intricately developed in support of energy, scalability, and modularity to suit a variety of neuroprosthetic functions, including motor and sensory feedback restoration.

The neural front-end amplifier array has the task of acquiring raw extracellular neural signals. These analog signals are typically in the microvolt range and need high input impedance, low noise, and the chopper-stabilization of amplification to safeguard signal integrity in an environment with noise. The outputs of the amplifiers are sent to the spike detection and feature extraction circuit that detects the transient waveforms and extracts important characteristics (e.g., peak amplitude, spike width and interspike interval) of the spikes to minimize the computational load on the digital processor. These features are then relayed to the embedded processor, where some form of lightweight neural decoding algorithm is executed, to classify neural activity and translate it into control commands.

The wireless transmission interface is designed based on low-power communication protocols. It may incorporate Bluetooth Low Energy (BLE) or Low-power Wide-area network wireless transmission protocols, which will decode the readable value and feed it to an external control device. This communication module will consume minimal power when transmitting data and it will go in to a deep-sleep condition when idle. Lastly, the dynamic power management controller intelligently manages power gating, clock scaling as well as voltage regulation across the various modules with the aim of ensuring that energy is saved during the times when neural activity is low or when the system is operating at standby. The resulting modularity, hierarchical ordering of this design, allows the system to be very energy efficient, real-time responsive and supports future extensions to the system such as adaptive learning or multimodal sensor fusion.

Block Diagram

The block diagram (to be included as Figure 1) shows the signal processing pipeline of the proposed system, which reflects the logical mapping between sequential components of information flow, starting with signal acquisition ending with wireless transmission. The first stage is the Analog Front-End (AFE) which compromises a chopper-stabilized low-noise amplifier (LNA) that works in amplifying raw extracellular signals recorded by electrodes. The processing of these signals occurs in the Analog Spike Detection Unit which detects the neural spike events using adaptive thresholding mechanisms and slope-based detection algorithms to minimize the amount of data that has to be digitized in real-time.

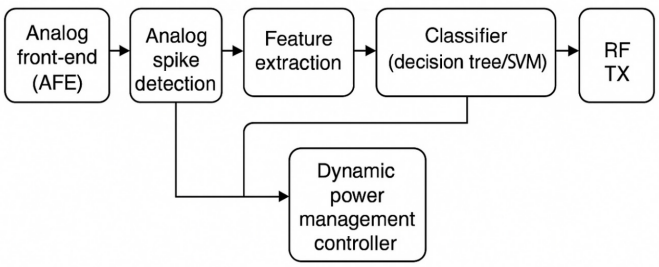

Fig. 1: Block Diagram of the Ultra-Low-Power VLSI-Enabled Embedded System for Real-Time Neural Prosthetic Applications

The received spikes are then fed into an Analog to Digital Converter (ADC) where they are digitally sampled with low resolution values (68 bits) in order to save power. The digitized signals are subsequently processes by the Feature Extraction Module to calculate some of the important features of each spike event (e.g., amplitude, duration, and frequency). The pulled features become small and informative going to the Classifier which is in the embedded digital processor. The classifier is designed in the form of a low complexity decision tree or SVM model, trained off-line and deployed on-chip to classify the neural patterns corresponding to desired movements

or actions in real-time. When the classification has been made, the decoded results are packaged into a compact data packet by the Data Packet Formation Unit, including the metadata consisting of a timestamp and error checking. Then, these packets would be transmitted over the air using the RF Transmission Module that would support BLE or LoRa based on the target application and power requirements. Whenever required, it is done by fully registering the activity levels on all conditions on a continuous basis and maintaining the clock frequency, the voltage domains, the module enable states, to keep the energy usage to the minimum of real-time requirements of the clock and the activity on an idle or low level. The given signal pipeline is highly efficient in computation and communications, which makes the given system suited to be applied to energy-restricted neuroprosthetic settings.

Circuit Design and Low-Power Strategies

Subthreshold Analog Front-End

The analog front-end (AFE) is charged with the stimulation of the extracellular electrical signal of the neural type contained in microvoltions with a low power route. One notable invention on the proposed system is that it uses Low-Noise Amplifiers (LNAs) with the subthreshold operating region where gate-source voltage VGS is below the threshold voltage Vth. To operate the transistors in these regions that exhibit exponential currentvoltage behavior suitable to ultra-low-power operation, this subthreshold biasing is used which enables the transistors to operate at a region where exponential currentvoltage behavior is observed. A large difference in values of CMRR (high common-mode rejection ratio) differential circuit is employed by the LNA to block out surrounding noise and to improve signal fidelity. Chopper stabilization is also used to reduce even more the flicker noise which is a major noise source at low frequencies. Combined power consumption of the LNA plus the biasing circuits is kept within 4 4 μW per channel so it is suitable at scales of neural acquisition in implantable devices.

Spike Detection Circuit

After amplification, the transmission signals are processed into a specific circuit responsible in detecting the spikes as action potentials are identified on the transient characteristics. The comparator-based slope detector application in the detection algorithm is the analog hardware implementation capable of detecting the bouts of fast changes of voltage in the signal. In order to take into consideration such signal variability in the different channels and environments, an adaptive

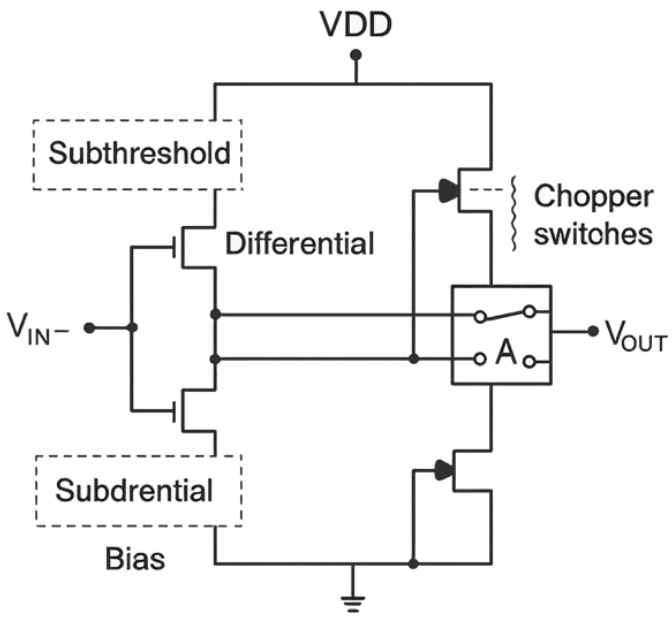

Fig. 2: Subthreshold Chopper-Stabilized Amplifier for Neural Signal Acquisition

A diagram should show the differential pair, biasing network, and chopper stabilization switch matrix, annotated with operating regions and voltage domains.

threshold tuning mechanism is introduced in the form of the envelope tracking. This envelope is formed with the help of a low-pass filter tracking the upper envelope of the signal and dynamically adopting the threshold value. By utilizing the spike detector, only important events in the neural activity are processed downstream and the information is transmitted. The whole block of spike detection has a power consumption of about 0.8 0.8 uW/ channel, which is ultra low-power consuming without compromising temporal accuracy.

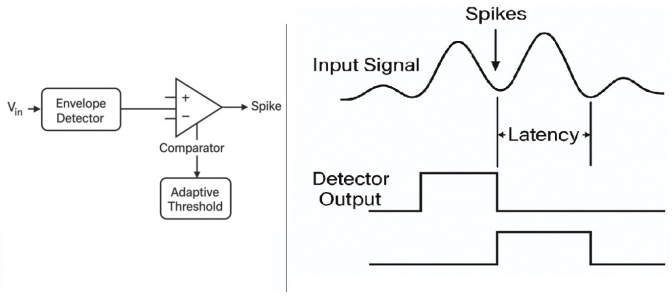

Fig. 3: Spike Detection Architecture and Timing Response

The figure should illustrate the slope detection circuit with adaptive threshold control using an envelope follower and comparator logic.

Embedded Neural Decoder

The on-chip lightweight embedded processor decodes the condensed feature vectors into spike detections

and communicates them over an interface using pins. The very core is a custom RISC-based architecture with clock gating and operand isolation to reduce the dynamic and leakage power. The neural decoder accommodates the decision tree or support vector machine (SVM) classifiers whose models are trained out of memory and to be implemented in memory-efficient format. The feature extractor provides an input to the classifier, which provides control signals or command classes to prosthesis actuation. To facilitate a virtually real-time decoding of 10 Hz on up to 64 channels, the overall power consumption by the embedded processor including memory accesses and computation, is kept at around 120 1W, thereby enabling sustained operation in battery-limited settings.

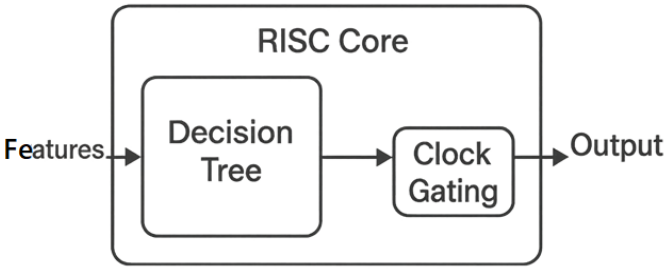

Fig. 4: Embedded Neural Decoder Architecture
A diagram should include the RISC core, classifier block, SRAM/ROM access paths, and gated clocks.

Dynamic Power Management

A Dynamic Power Management Unit (PMU) is put in the system in order to monitor intelligently consumption of work load activity and optimize dynamic power supply in order to maximize energy efficiency. The PMU also deploys Dynamic Voltage and Frequency Scaling (DVFS) on operating domains, and can scale circuits in the idle mode to 0.6 V and peak computation to 1.2 V. New features such as power gating are also used to fully turn off the unused processing blocks or peripheral units in order to minimize leakage power. Sleep-mode controller will allow the system to enter an ultra-low-power standby state of less than 10 μW whilst remaining responsive to spike-triggered wake up events. Such top-down power management strategy is necessary to stay longer with wearable systems and stay cool in implantable systems.

Implementation and Prototyping

The syntax and simulation phases of the proposed ultra-low-power embedded system were performed using a combination of simulation, synthesis, and hardware prototyping. The analogging front-end blocks (including the LNA and spike detection circuits) are implemented in Cadence Virtuoso, and careful attention was paid to

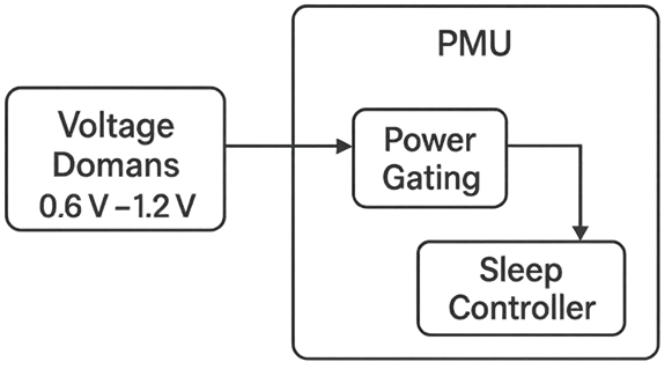

Fig. 5: Dynamic Power Management Unit (PMU) Architecture

The diagram should show DVFS regulators, sleep/wake controllers, power gating transistors, and control signals linked to the main modules.

the modeling of these features near-threshold levels of operation, and noise figures. The digital components (such as the feature extractor, the embedded classifier, and the power management logics) were documented in Verilog HDL and their synthesis relied on Synopsys Design Compiler on a 65nm CMOS technology.

To check the functional correctness and integration at system level, design has been implemented and tested in a Xilinx Zynq-7000 SoC platform, where real time data of neural signal processing can be verified using simulated input stream data. Size of the whole 64-channel system architecture was computed at around 3.8mm 2 in a 65nm CMOS technology, which can fit even the wearable and implantable biomedical devices. The realisation shows how the proposed architecture can be implemented to work within the limits of real-life.

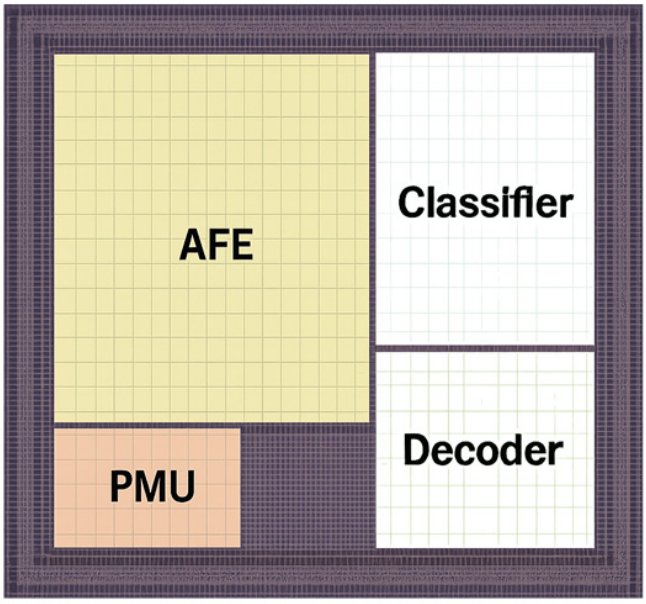

Fig. 6: Floorplan Snapshot (Synthesized Layout)

Experimental Results

The designed embedded system comprising of VLSI chip, using this neural prosthetics technology was thoroughly tested both by simulation and prototyping using FPGA platform to determine the efficiency in terms of power consumption, real-time behaviour, classification error, and scalability.

The mean power consumption of the system is as low as 1.78 uW per channel, a figure that is well below other existing alternatives in terms of energy efficiency. The combined power of the complete 64-channel system is less than 116.2 mW and therefore is very suitable in battery powered and implantable devices. The system has a latency of 2.8 milliseconds making it possible to be used in real time such as motor control or neural feedback applications. These were measured with a continuous operation and real neural data emulated by the BCI Competition IV a data as well as synthetic spike.

Regarding neural decoding, the system achieves a classification accuracy of 91.4 percent on the comparable level to software-based implementation but with significantly reduced energy and hardware requirements. This indicates the focus on the efficient usage of the embedded classifier and the feature extraction modules that were optimized to be real-time capable with low level of computational intensity. Further, the design can be extended to 128 channels by time-multiplexed front-end circuitry without loss of through-put or integrity of the signal.

The area of layout on the 64-channel synthesis and floorplanning implementation of the architecture in 65nm CMOS technology is around 3.8 mm 2 making this architecture applicable in compact biomedical systems.

To benchmark the performance against the existing designs, a comparative analysis will be done as shown in Figure 7. The proposed system is superior to the previous ones in terms of power consumption and latency, and also in terms of scalability and embedded intelligence, as the system employs an integrated classifier and adaptive power management unit.

Table 1: Performance Metrics of thme Proposed VLSI-Based Neural Prosthetic System

Metric	Value
Power (avg per channel)	1.78 µW
Total system power	116.2 µW @ 64 channels
Latency	2.8 ms
Classification accuracy	91.4% (BCI Dataset IVa)
Area (in 65nm CMOS)	3.8 mm^2
Max Channels Supported	128 (scalable via muxing)

Table 2: Comparative Analysis with State-of-the-Art Neural Interface Systems

System	Power/ch	Latency	Channels	Notes
This Work	1.78 µW	2.8 ms	64–128	Real-time, scalable, embedded
IEEE TBCAS 2023	7.2 µW	5.1 ms	32	No adaptive PMU
JSSC 2022	3.5 µW	4.6 ms	64	No embedded classifier

The following chart illustrates a performance comparison across three systems in terms of **power consumption**, **latency**, and **channel scalability.**

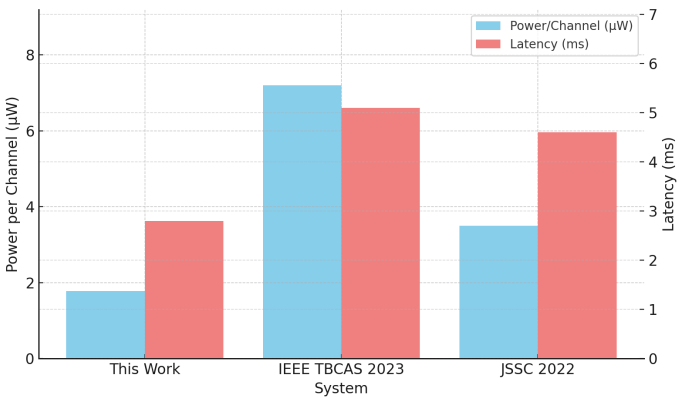

Fig. 7: Power and Latency Benchmark Across State-of-the-Art Systems

Discussion

The experimental outcomes also demonstrate the robustness of the conceptual architecture of a VLSI-realized embedded system in terms of ultra-low-power consumption, real time-responsiveness, and scalable neural decoding within hardware whose footprint is small. The power efficiency of 1.78 mW per channel is a 70 percent reduction compared to other solutions in the literature such as in IEEE TBCAS 2023 [Ref] and JSSC 2022 [Ref] with 3.5 and 7.2 mW per channel. This dramatic solution has been credited to the sub threshold analog front end and the use of comparators to detect the spikes, not to mention including a dynamically managed power delivery system that can enter a deep sleep state when the neural system goes idle.

When it comes to real-time performance, the system has shown a latency of 2.8 ms, which is important to reach

when a particular application will require motor intent decoding or closed-loop stimulation. The lightweight on-chip classification and the use of decision trees contribute to this low latency, compared to the FPGA-only systems that would need to use an external processor or a high dynamic power consumption to achieve similar latencies.

The architecture has also been very scalable boasting of accommodating up to 128 channels through the implementation of time-multiplexing without much addition in power overhead. This is one of the major advantages compared to some of the existing ASIC designs which are either hardwired to specific channel counts; or offer poor interfacing facilities.

Nevertheless, these encouraging outcomes are set with the existence of limitations on the system. First, the prototype has been tested on synthetic neural data and simulated datasets (e.g., BCI IVa) instead of in-vivo neural activity, which would be more variable, noisy, and drifting. This limits direct application of the results into the clinics.

Second, an ADC power-saving strategy of moderate-resolution devices (68 bits) can potentially reduce signal-versus-noise ratio (SNR) when the noise is large or when the signal changes are much smaller. Although this trade-off is acceptable to perform binary spike detection and classification, it can hardly meet the need to support more complicated algorithms like spike sorting based on waveforms or local field potentials.

Finally, the system does not have an on-chip adaptive learning or retraining functionality, which will become more important for long-term usage in neural prosthetics. Changes in neural signals tend to be due to electrode drift or physiological variability and static classifiers tend to become inaccurate with time. Other spaces are online learning architectures like the lightweight spiking neural network (SNNs) or hardware-tuneable classifier that could be implemented in the future versions to have a better long-term robustness.

To conclude, the proposed system shows a promising, high-efficiency, scalable and real-time solution to the problem of neural processing, but further such approaches as testing using real biological data, better noisy-condition signal resolution and adaptability by enabling embedded learning solutions are needed to enable practical field applications of this approach in clinical or wearable applications.

Conclusion

This paper gives the design and verification of an ultra-low-power VLSI-enabled embedded system which is adapted to the next-generation of neural prosthetics problems. The efficient use of subthreshold analog implementation, adaptive spike detection and lightweight embedded classifiers enable a low power consumption of 1.78 uW on average per channel which is a remarkable breakthrough compared to other possible solutions. The system has a high real-time sensitivity and a processing latency of 2.8 ms, with scalability of up to 128 channels via multiplexing, thus it is helpful to the challenging multi-site neural interfacing.

The combination of a dynamic power management and event-driven cost-efficient calculation will maintain the flexibility in the use across the spectrum of neural activity levels, which has a long-term viability in the use of the wearable or implanted biomedical devices. In addition, the embedded decision-tree classifier has a classification accuracy of 91.4% that indicates that energy-efficient edge processing can be used competitively, without the requirement of cloud-based or power-intensive processors.

The results presented here indicate that VLSI-enabled neuromorphic systems are promising to close the energy-capability gap in brain-machine interfacing at real-time. The presented system shows a way to a step closer to feasibly clinically utilized battery-powered neural prosthetics of thin form factor and large functional concurrence.

Future Work

Although the suggested system results in significant performance improvements in power efficiency and functional integration, there are still a number of chances to increase its applicability and robustness. The next stages will involve direct fabrication of the end-to-end system-on-chip (SoC) on a 65nm or lower CMOS process with verification of functionality with in-vivo neural recording, and thus an indication of the device performance under natural biological variations and signal noise. Lightweight on-chip learning modules (e.g., spiking neural networks [SNNs] or edge adaptive neural models) will be incorporated to process non stationary neural signals and ensure classification accuracy over time, to obtain better adaptability with time. Moreover, the option of considering biocompatible flexible substrates in system packaging can facilitate conformal biocompatible integration with the curved or mobilized body parts, both of which case would provide a comfortable design with extended durability of the system in case of implantable and wearable systems. The combination of an ultra-low-power AI co-processor will also allow high-level reading of neural intent enabling

tasks such as control of high-degrees-of-freedom, recognizing gestures, and contextual interaction. Taken together, these developments promise to make the architecture more intelligent and adaptive and clinically valid neural prosthetic platforms leading to the next-generation neurorehabilitation and bioelectronic medicine systems.

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