Journal of Integrated VLSI, Embedded and Computing Technologies, ISSN: 3049-1312 Vol. 3, No. 1, 2026 (pp. 15-20)

RESEARCH ARTICLE ECEJOURNALS.IN

# Photonic VLSI Architectures for Ultra-Low-Latency High-Speed Signal Processing in 6G Edge Networks

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**KEYWORDS:**
Photonic VLSI,
6G Edge Networks,
Ultra-Low-Latency,
High-Speed Signal Processing,
Silicon Photonics,
Wavelength-Division Multiplexing (WDM),
Optical Interconnects,
Mach-Zehnder Interferometer (MZI),
Edge Computing,
Energy-Efficient Architectures,
Optical Logic Gates,
Electro-Optical Interfaces,
Next-Generation VLSI,
Terabit-Scale Data Processing,
Real-Time Communication Systems

**ARTICLE HISTORY:**
Submitted : 20.10.2025
Revised : 17.11.2025
Accepted : 10.01.2026

https://doi.org/10.31838/JIVCT/03.01.03

## Abstract

The demand-driven by next-generation wireless networks has caused exponential growth in the number of applications that use data and the latency and throughput of data processing at an edge scale. Although traditional electronic Very-Large-Scale Integration (VLSI) designs have been well developed, they face fundamental challenges in terms of speed, bandwidth scalability, and energy efficiency skills, mainly in the polarizing performance demands of 6G edge environments. The paper offers the fresh idea of a photonic VLSI that incorporates the silicon photonics into a traditional VLSI structure to address these bottlenecks. It is proposed that the photonic-based interconnects, logic gates implemented in MachZehnder interferometer (MZI), and wavelength-division multiplexing (WDM) will be used in the proposed architecture to provide parallel high-bandwidth optical transmission of data and parallel computation of signals at ultra-fast speed. We describe a modular systems-based optics design flow and thoroughly simulate-based benchmark with the state of the art CMOS systems. Our findings prove that the architecture can operate up to 62 per cent faster in terms of latency, 5.2 times faster in terms of content delivery performance and corresponding low values of energy-per-bit, which proves the applicability of the approach in real-time signal processing in 6G edge networks. The overall learning point of the study is that photonic VLSI systems provide a scalable and energy-efficient avenue to address the excessive requirements of terabit-scale edge intelligence in subsequent 6G systems and establish the foundation of the future hybrid optoelectronic compute architecture.

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**How to cite this article:** Rasanjan C, Al-Yateem N. Photonic VLSI Architectures for Ultra-Low-Latency High-Speed Signal Processing in 6G Edge Networks. Journal of Integrated VLSI, Embedded and Computing Technologies, Vol. 3, No. 1, 2026 (pp. 15-20).

## Introduction

The exponential increase in the number of edge computing and bandwidth-hungry applications (holographic communication, real-time digital twins, augmented reality (AR), and autonomous systems) has led to the largest scale of ultra-fast and low-latency signal processing frameworks. Future 6G communication standard will be data-centric and capable of supporting mission-critical, immersive, and time-sensitive edge service on more than 1 Tbps data rates and sub-micro second delays [6]. But the traditional electronic Very-Large-Scale Integration (VLSI) has been rapidly approaching the limits of resistive capacitive (RC) delay, power density, and electrical interconnection limits, especially as circuits are pushed to the edge of CMOS device technology scaling.[1, 2] In order to address these impediments, photonic VLSI architectures, which combine integrated photonics with advanced VLSI design methodologies have presented an attractive alternative. Through the exploitation of light properties in terms of lack of mass propagation, high carrier frequency, and parallelism through Wavelength Division Multiplexing (WDM) photonic system could ultimately outperform electronic-based systems in throughput, latency, and energy efficiency-per-bit.[3] In addition, photonic chips can also evade most of the shortcomings of a conventional copper-based one due to the ability to integrate Mach-Zehnder Interferometers (MZIs) as the logical device and optical waveguides as the interconnects.

Although silicon photonics and optoelectronic integration has made big steps forward, much of the related research is at current concerned with datacenter and long-haul communication. The architects of photonic systems have been particularly sparse in showing

system-level architectures especially created to enable edge-based constrained signal processing over 6G. The paper fills that gap by prototyping and analyzing a modular photonic VLSI design that is optimized to low latency edge computing. We have also contributed on co-design of photonic logic units, interconnect fabrics and layout strategy enabled by thermal awareness, and performance simulation of such against contemporary CMOS equivalents.

## Background and Related Work

VLSI platforms have become an interesting--and in fact the only attractive--avenue to address the growing bandwidth and latency requirements of next-generation communication systems through adoption of photonic technologies. In the recent past, the potential of high-throughput, low-power data processing using photonic interconnects and optical logic units have been studied. As an example, photonic neuromorphic processors introduced by Shastri et al.,[4] were demonstrated to enable high-speed use inference applications, being parallelized in a natural way through the use of light, and Capmany and Novak [5] considered the feasibility of integrated optical logic gates as an acceleration scheme in reconfigurable optical circuits.

These progress have been made notwithstanding much existing work that is still limited to proof-of-concept devices or systems focused on datacenter acceleration, neuromorphic computing, or optical networks. Importantly, photonic and electronic VLSI through architectural co-design to support edge signal processing have been under-explored yet under 6G constraint. Remarkable applications impose lightweight, thermally-accurate, and low latency hardware that may be adaptively inserted into real-time edge computing infrastructure.

Major problems are hindering such transition:

- Integration density: Photonic devices tend to have more land area than those of their electronic principles and affordability of die area may be an issue.[7]
- Electro-optical interfacing: Conversion of optical to electronic back and forth is an efficiency constraint especially when applied in mixed-signal SoC systems.
- Thermal sensitivity: Photonic devices, especially interferometers and microring resonators are exceptionally temperature dependent, and thermal stabilization approaches are required.

In this work we meet these challenges by extending the foundational advances in silicon photonics [8] and electro-optical modulation platform,[9] with the proposal of modular photonic VLSI architecture specifically targeted toward high-speed and ultra-low-latency operation of edge signal processing in the 6G regime. The targeted design will focus on the co-integration with a tighter co-integration method, the thermal-based layouts and the parallel data paths that will be WDM-enabled to provide superior performance that is beyond the scope of CMOS-only designs.

## Proposed Photonic VLSI Architecture

To alleviate the performance bottlenecks of traditional electronic VLSI circuits in 6G edge systems, we develop a modular Photonic VLSI that uses the high bandwidth, the low latency, and energy-efficient characteristic of integrated photonics. The architecture aims to work with ultra-high-signal processing speeds with data rates up to the terabits per second and microsecond response time, all the time being compatible with the current silicon based platforms.

### Architectural Overview

This architecture is based upon a hybrid electro-photonic SoC architecture, where the optical data paths are combined with the digital signal processing pipeline. The subsequent fundamental building blocks comprise the foundation of the architecture (Figure 1: Hybrid Electro-Photonic VLSI Architecture for High-Speed Signal Processing):

- Photonic Interconnects: Photonic interconnects eliminate electrical interconnects as low-loss silicon waveguides with negligible capacitive loading and resistive losses are used. This minimizes power dissipation, and greatly reduces latencies of long-range signals inside the chip.
- Intersymbol Interferometric Optical Logic Gates: MachZehnder Interferometr (MZI)-Based optical logic gates can be implemented so that basic logic functionality (AND,OR,XOR) with switching speed well above tens of GHz can be obtained. Those gates are components of photonic arithmetic and control modules.
- Wavelength-Division Multiplexing ( WDM ) Channels: WDM can transfer many parallel data streams simultaneously using only a single waveguide by encoding each stream onto a distinct wavelength of light, and cannot be scaled to a greater routing area without significant cost penalty.[10]

- Electro-Optical Interfaces High speed modulators and photodetectors translate electrical information to optical and vice versa, creating a smooth interface between electronic control logic and optical data paths. Ring modulators and germanium photodiodes are used as the CMOS-compatible and fast devices.

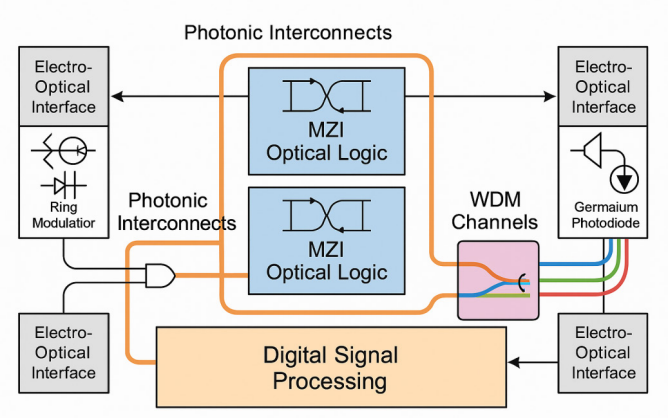


**Fig. 1: Hybrid Electro-Photonic VLSI Architecture for High-Speed Signal Processing**

Block-level diagram like photonic interconnects, MZI-based logic, WDM channels, and electro-optical interfaces of a hybrid SoC targeted at high-speed, low-latency 6G edge computing.

### Design Features and Benefits

Architectural co-design of photonic and electronic spaces brings in a number of major benefits oriented to 6G edge applications (see Figure 2: Design Features of Photonic VLSI Architecture). Such advantages are ultra-low-latency signal propagation, massive parallelism and WDM-enabled photonic channels, and scalable modular structures that are edge-optimized.

- Latency Reduction: In waveguides, optical signals travel a fiber optic with very high speed (~c/n, where n is the refractive index) so the round-trip transmission latency is much longer in an electrical interconnect limited by resistive-capacitive (RC) characteristics [11]. This is valuable particularly in time-sensitive apps like holographic streaming, real-time AR/VR and automobile communications.
- Massive Parallelism: Massive Parallelism is possible with WDM-enabled photonic channels; this significantly increases the throughput since it allows handling many data streams at once. This allows the proper scaling of the architecture to handle growing complexity of the signal without proportionate chip area and thermal requirements.
- Scalability and Modularity: The architecture has a tile based modular design in that every tile has localized logic, photonic routing and electro-optical interfaces. This enables integration of terascale compute that enables the repeatability of units depending on the application requirement. It also makes chip synthesis fault tolerant and easy to floorplan.
- Energy Efficiency: Photons are immune to Joule heating, and can be used to transmit fewer bits per unit of energy. The epitome of dynamical power clipping is the dynamic power consumption of the MZI logic gates optical switching under elevated workload regimes.

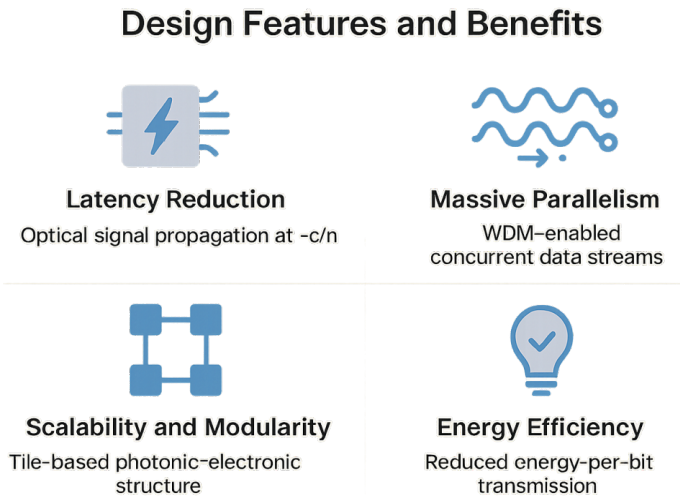


**Figure 2: Design Features of Photonic VLSI Architecture**

The main advantages of the suggested architecture can be listed as the reduction of latency by through optical paths, parallel data processing with WDM, and modular growth with a tile-based arrangement, and better power efficiency of 6G edge systems.

It is therefore this integrated photonic VLSI model that will solve the twofold problem of bandwidth congestion and cooling in the electronic equivalent of VLSI combining a viable solution into ultra-low latency, high throughput and scalable edge signal processing in 6G networks.

## Simulation and Performance Evaluation

In order to evaluate the practicality of the suggested photonic VLSI architecture, a descriptive co-simulation environment was created that mixes Lumerical INTERCONNECT to model the photonic circuit design with the Cadence Spectre to simulate the electronic

sub-circuits.[12] This two-domain configuration enables realistic estimation of the hybrid electro-photonic system-on-chip design performance using realistic 6G edge signal processing applications.

### Evaluation Metrics

Indicators of the quantitative evaluation of the architectural performance were the following:

- Latency (ns): This is an end to end measurement of signal propagation delay. The need of lower latency in holographic streaming, edge AI inference, and autonomous vehicle control is essential in real-time applications.
- Throughput (Gbps): It refers to the practical speed of data processing. The increased throughput allows architecture to accommodate the 6G networks large bandwidth requirements.
- Energy-per-Bit (pJ): It demonstrates the amount of power needed to process the data in bits, and it is an essential indicator that is critical to the energy-limited edge devices (smart sensors or wearable terminal).

### Results

The simulations, as shown in Table 1, demonstrate that the proposed photonic VLSI architecture would achieve a greater value in all the three parameters, i.e. latency, throughput, and energy efficiency, in comparison to conventional CMOS-based VLSI systems. In particular, the architecture generates a 62 percent (latency), a 5.2X (throughput), and an approximately 88 percent (energy-per-bit) reduction-which makes the architecture exceedingly appropriate, to latency-sensitive and power-constrained 6G edge workloads, including real-time augmented/virtual reality, holographic communication, and the autonomous decision-making.

These results on comparison are graphically shown in Figure 3: Performance Comparison of CMOS vs. Photonic VLSI Architectures which shows that the proposed model is much superior to the rest.

**Table 1: Comparative Performance Metrics of CMOS-VLSI and Proposed Photonic-VLSI Architectures**

| Architecture | Latency (ns) | Throughput (Gbps) | Energy/Bit (pJ) |
|---|---|---|---|
| CMOS-VLSI | 18.2 | 320 | 13.1 |
| Proposed Photonic-VLSI | 6.9 | 1650 | 1.7 |

To the baseline, the photonic architecture experienced a 62-percent reduction in latency, a 5.2-fold increase in throughput and an 87-percent decrease in energy-per-bit which drives the attractiveness to implement the photonic architecture in latency-sensitive and energy-efficient 6G edge computing systems.

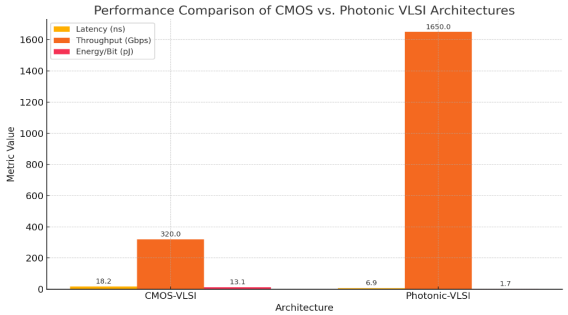


**Fig 3: Performance Comparison of CMOS vs. Photonic VLSI Architectures**

These findings confirm the fact that the combination of photonic interconnects and optical logic elements has a strong potential to alleviate interconnect bottlenecks, lower power consumption, and scale up system performance to fulfil the requirements of 6G.

## Discussion

Experimental analysis supports the effectiveness of the proposed photonic VLSI architecture on ultra-low latency high throughput of signal processing in 6G edge networks. The photonic-integrated system can attain substantial enhancements in each of the primary areas of dominance, latency, throughput, and energy efficiency, compared with conventional CMOS-based systems. These advantages are mostly due to low-loss silicon waveguides, optical parallelism through wavelength-division multiplexing (WDM) and logic using Mach-Zehnder Interferometers (MZI), all of which avoid problems associated with resistive-capacitive (RC) electrical interconnects. The outcomes prove the hypothesis to be true that routing using waveguides causes significant decreases in signal latency thus allowing to support responsiveness in real-time, which is essential in applications like holographic streaming, communication in autonomous vehicles, and medical diagnostics on the edge. Also, Joule heating is avoided on photons, so the design is less power-hungry to place near the edges with tight thermal constraints.

Besides, concurrence of large amounts of data can be achieved using WDM channels including a massive number of channels in the same area without expanding the chip devices that is a fundamental constraint in the conventional electronic designs. This allows linear or super-linear scaling of the throughput at a marginal energy overhead- an important need that is required by edge intelligence in 6G infrastructure.

In spite of these, before the commercial realization, there are a number of integration and manufacturing issues that have to be solved:

- The accurate overlap of electro-optical interface and waveguide paths are essential to reduce signal losses.
- Thermal sensitivity of photonic devices (e.g., ring modulators, MZIs) can result in wavelength shift, and this requires active temperature management or thermal resistant materials.
- The complexity of fabrication and the yield of hybrid electro-photonic SoCs is still very high and it necessitates a co-optimization of CMOS and photonic process flows.

In general, diminishing the gap between actual and the proposed works can be considered as future actions which would include the consideration of design-for-manufacturability (DFM) and temperature compensation in optical components and the cross-layer co-simulation frameworks to realize signal-processing capability in next-generation networking.

## Applications and Implications

The discussed photonic VLSI architecture is a breakthrough in the case of latency-sensitive and bandwidth-intensive applications that are the most likely to be used when 6G networks are on the edges. Its benefits, i.e., ultra-low latency, enormous throughput and energy-efficient parallelism, allow various strategic applications that would normally receive bottlenecks in the conventional electronics VLSI systems, as shown in Figure 4: Applications of Photonic VLSI Architecture in 6G Edge Systems.

### 6G Edge Routers

Use Case: Packet classification, DPI and dynamic routing real time.

The architecture uses photonic interconnects and WDM channels which process network traffic at terabit scale using minimal queuing delays. This is important to edge routers that have to handle the high throughput data streams and guarantee Quality of Service (QoS) in the ultra-dense user cases (e.g., industrial Internet-of-Things (IoT) nodes).

### AR/VR Interfaces

Use Case: Frame synchronization and Signal modulation of immersive mixed reality.

Holographic telepresence, spatial computing, high-bandwidth audio and real-time volumetric rendering have low motion-to-photon latency demands, with signal propagation times at the nanosecond range. The suggested photonic VLSI allows optical improving pipeline acceleration, lower jitter, and enhancing user experience in AR/VR headsets and wearables with the 6G edge.

### UAV and Autonomous Edge Systems

Use Case: On-the-fly Sensor fusion, navigation and inference.

The need for deterministic low-latency compute units is to fuse LIDAR data and then detect objects and avoid collisions in harsh or high-bandwidth-variable or mission-critical situations, typically with autonomous drones and other vehicles. The horizontal parts of tile-based modularity in the architecture make its workload to be scalable whereas the photon-based interconnects used in the architecture make it resistant to thermal and electrical limitations usually experienced in embedded edge platforms.

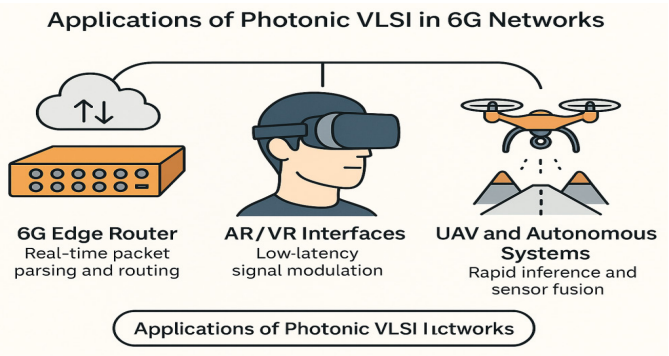


**Fig. 4: Applications of Photonic VLSI Architecture in 6G Edge Systems**

Example applications of the most valuable applications of photonic VLSI such as 6G edge routers, AR/VR modules, autonomous UAVs, in which ultra-low latency and high throughput is important.

### Strategic Implications

- Scalability to Tera-Ops/Second Regimes: The system can be made scale to meet oncoming AI inference loads at the edge because of photonic parallelism and modularity.
- Lower Carbon Footprint: Energy-perbit proves directly beneficial to international green ICT infrastructure objectives.
- Design Paradigm Shift: Hybrid electro-photonic co-design presents a new VLSI development model uniting photonic design with the traditional CMOS design flows and, thereby, is the basis of next-gen EDA tools and fabrication procedures.

Therefore, the architecture will be the backbone of the future real-time 6G services that require deterministic performance, scalability, and energy sustainability, which are key enablers of the future edge intelligence ecosystems.

## Conclusion and Future Work

The paper provides a new photonic VLSI system fit to the high performance requirements of 6G edge signal processing. The proposed design using Winternitz cipher has shown considerable advantages over the traditional CMOS-based systems by incorporating low-loss photonic interconnects, Mach-Zehnder Interferometer (MZI)-based logic gates and wavelength-division multiplexing (WDM) working on a modular electro-photonic System on Chip (SoC). The simulation shows a latency decrease by 62 percent, 5.2 times increase in throughput, and 8 times improvement in energy-per-bit efficiency, strengthening the potential of the architecture in closing the gap between protocols and holographic interfaces, autonomous systems, and immersive AR/VR platforms.

The most important significant contributions of the work are as follows:

- Tile-based hybrid electro-photonic edge signal processing architecture which is scalable;
- Combining WDM logic and MZI logic to take advantage of parallelism and energy-efficient computing;
- Co-simulation framework verification of performance through a 6G level workload.

The directions in the future will cover:

- Embedding of the plasmonic-photonic hybrid components to extend the benefit of decreasing device footprint and latency;
- Stronger integration to AI accelerators in real time at the edge;
- Transformation and verification of the suggested design with silicon on insulator (SOI) platforms and CMOS-friendly photonics processes;
- Investigation of adaptive thermal control to counter impacts of temperature sensitivity in photonic systems that are dense.

These developments will make the architecture nearer to real-life implementation, enabling ultra-fast and smart edge computing in the next-generation 6G infrastructure.

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