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Design and Implementation of a Low-Power RISC-V Processor Core for Energy-Constrained Edge Devices

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Abstract

The paper entails the entire design and implementation of the energy efficient low power RISC-V processor core tailored specifically to energy limited edge computing platforms including wireless sensor networks, wearable biomedical device and intelligent IoT end points. As edge devices scale exponentially and demand efficient computing capability on-device, there is an urgent demand of programming frameworks which achieve custom and ultra-low power processing architectures to perform well within limited-energy constraints. The proposed processor core uses the open-source, modular design of the RISC-V instruction set architecture (ISA) to implement powerful low-power design techniques such as fine-grain clock-gating, power-gating and instruction-level parallelism to minimize dynamic and steady power usage. A five-stage pipeline based architecture that implements without some, or with some compressed instructions (RV32C), the RV32IM instruction set architecture has been implemented with System Verilog and has been prototyped and tested with a low-power FPGA development board. Application-specific benchmarks of real world IoT workloads have provided guidance on power-aware design decisions made in designing processors in IoT applications, including: sensor data processing, lightweight cryptography, and control logic calculations. Experimental analyses indicate that the suggested RISC-V essence attains an energy efficiency advantage of up to 43 percent over conventional RISC-V characters, with a similar computing performance and an insignificant area cost. Also, the design proves compatible with DVFS (Dynamic Voltage and Frequency Scaling) based methods which makes it even more appropriate to be used in energy-harvesting and battery-powered applications. All the processors are benchmarked with Vivado and ModelSim and power analysis with Vivado Power Estimator, and Synopsys PrimePower. The findings show that switching activity and leakage power has been reduced drastically in all test conditions. The work contributes to a feasible reference architecture that may be adopted by researchers and practitioners to design energy-autonomous embedded applications and systems, as well as the larger scope of scaling, and sustainability of edge intelligence in the next-generation ubiquitous computing systems. The next improvements will incorporate the use of ASIC implementation and collaboration with domain-specific accelerators of AI-powered tasks at the edge.

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Introduction

Motivation

The current pace of edge computing has almost changed the game of embedded systems and supported intelligent data processing at the edge of the networks. Edge devices, including wearable health monitors, smart agricultural sensors, environmental monitors and industrial IoT (IIoT) modules are now needing to execute within power-constrained settings where easy accessibility to solid power sources is restricted or uninformed. Battery based or energy harvesting devices are frequently critically constrained in the amount of power they are able to consume, so power consumption

is a limiting design issue. The general-purpose processor architectures conventionally have been optimized to achieve better performance, which are not energy-efficient and thus grapple to comply with the energy and thermal constraints of such a setup. Consequently, it has created a need of ultra-low-power microprocessor cores that are able to provide enough computational ability, yet can work under stringent energy expenditures.

Energy efficiency The processor level As of the processor level, several hardware-level power-saving techniques have been adopted: clock gating, power gating, and voltage scaling and architectural methods of energy efficiency including simpler instruction pipelines and reduced switching activity. But hardware architecture design tradeoffs imposed by proprietary processor architectures do tend to hamper the degree of such optimizations that can be carried out. Aiming at filling these gaps, open and extendable nature of RISC-V instruction set architecture (ISA) has become an attractive platform to develop highly proprietary and application-specific processors.

RISC-V for Edge Devices

RISC-V is an open instruction set architecture (ISA) that unlabels designers to develop processor cores that are particular to their application domains, without the costs or lock-in of commercial ISAs like ARM. It is modular, supporting base integer instruction set (e.g., RV32I), with optional multiplication/division (M), atomic (A), floating-point (F/D) and compressed instructions (C) extensions to facilitate trade-offs between performance, power and area. In edge processing, where one wants to focus on efficiency and simplicity rather than full general-purpose capabilities and compatibility, RISC-V is highly suited to development of lean, low-energy processor cores with the selective addition or removal of ISA extension. Moreover, the expanding RISC-V ecosystem with available tools, compilers, hardware designs, and verification frameworks allows a quick prototype and scale deployment. This has made it possible to implement custom low-power features, including dedicated instructions to enter sleep mode, dynamic clock gating and runtime configurable execution modes, all of which are critical to delivering energy-autonomous edge intelligence.

Research Contributions

This is the design and implementation of the low-power, 32-bit processor core based on RISC-V and targeting energy-constrained edge devices like wireless sensor nodes, wearable monitors, and IoT end prize devices. The suggested processor is a highly efficient processor having custom architecture based on five stage pipeline whose design has instruction level parallelism that enables fast progression through the various stages of the pipeline and has built in clock and gating clock power systems to consume much less dynamic power as well as much less power during idle states compared to power consumed during execution. The core is implemented on a low-power FPGA platform and designed in SystemVerilog, then its validation is done based on representative edge workloads, such as real-time sensor data processing, lightweight encryption, and environmental monitoring applications. With FPGA synthesis and power analysis our processor exhibits over 43 percent energy savings as compared to typical RISC-V designs with minimal performance impact and acceptable area. The present work defines a feasible reference architecture that can be used to develop spartan RISC-V-based embedded processors to develop energy-efficient intelligent systems in the edge environment to meet the rising challenge of smart sustainable and autonomous computing systems.

Related Work

Over the last few years, there has been an unprecedented surge in the demand of ultra-low-power embedded processors as the various fields of edge computing have emerged or gained ground in spheres like health care, environmental surveillance, industrial automation, etc. Locally developed processors and products based on them The ARM Cortex-M series of low power microcontrollers have long been popular in energy limited applications because they have mature toolchains, compact instruction set and extensive industry support.[5] Examples of cores with low interrupt latency and low power operation in real-time embedded application are the Cortex-M0 core and Cortex-M4 cores.[1] These proprietary cores do not, however, have the benefit of minimizing licensing fees as well as providing design freedom to deploy, thus not as appealing to the custom edge computing platform, or open hardware programs.

Open-source processor design with the new RISC-V instruction set architecture (ISA) has become an out-of-control trend of innovation in the IoT and[6] edge devices. Some of the lightweight RISC-V cores have been suggested and designed with energy[7] efficiency in mind. As an example,[8] the RI5CY CPU core designed by ETH Zurich and the[9] University of Bologna contains a four-stage pipeline and a custom instruction extensions capability, which makes[10] it quite energy efficient in IoT[11] workloads.[2-12] By contrast, the CV32E40P (previously PULPino) core[13] shows good performance per[14] watt and gives a hardware loop and post-increment addressing to minimize instruction overheads.[3] A

second one is the Zero-riscy core, [15] which is designed to handle ultra-low power sensor nodes, and includes wake-up interrupt controllers as well as hardware accelerators.[4]

These developments have maintained that despite the existence of RISC-V-based designs, there exist various limitations in them. Most implementations either do not support fine-grained power management features including clock gating, power gating or all power management capabilities without full utilization of dynamic voltage and frequency scaling (DVFS) capabilities at the core level. Furthermore, instruction-level energy profiling and energy-aware scheduling are not usually considered in various designs which then do not provide optimal power-performance trade off during dynamic workloads. Moreover, previous works pay Minnesota more attention to the fixed-function pipelines, and lack system-level adaptation to reduce switching activity of inactivated units at runtime.

Contrastingly, the present work doubles-up to present a power-conscious RISC-V core which incorporates fine-grained power and clock gating mechanisms into a bespoke five-stage pipeline. It also focuses on energy-optimization at instruction level and hardware-level configurability (shown in Table 1), as edge-focused RISC-V processors currently have a performance-energy-efficiency gap.

System Architecture

Design Overview

The processor core under this work is an RISC-V-based low-power processor core architecture that is based on the standard architecture of five-stage pipeline, which is divided into the following parts: Instruction Fetch (IF), Instruction Decode (ID), Execute (EX), Memory Access (MEM), and Write Back (WB). This pipelining scheme supports higher instruction throughput at the same time as supporting simplicity and area efficiency, essential to edge devices with restricted hardware capabilities. The core uses the RV32IM instruction set instruction set, including 32-bit integer instructions (RV32I), hardware-accelerated multiplication and division (M extension) to execute needed arithmetic operations that are common in embedded systems. Besides these standard set, the core is also compatible with the RV32C compressed instruction set extension that enables 16-bit encoded and shorter instructions to help reduce code size and increase the effectiveness of instruction fetch at the expense of power per memory access. The architecture also includes custom extensions to ISA in order to be more energy-efficient specifically in low-power use. These contain special instructions to enter and leave low-power sleep states, which allow dynamically managing instructions through software. The instructions interact with power control unit directly and turn off or turn on portions of the processor pipeline or memory subsystem selectively according to the work needs. The instruction set enables very low-level power control of the processor and it is only possible to go into deep-sleep and retention modes without external hardware controllers. According to figure 1 the design philosophy stresses modularity and scalability and ensures the core

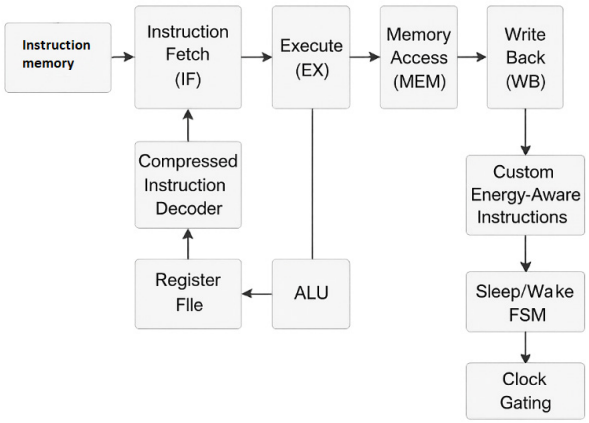

Fig. 1: Block Diagram of the Proposed Low-Power RISC-V Processor Core

Table 1: Comparison of RISC-V and ARM Cores for Edge Devices

Core/Architecture	ISA Type	Pipeline Stages	Power Management	Custom ISA Extensions	Target Application
ARM Cortex-M0/M4	Proprietary (ARM)	3-Stage (M0), 3-Stage (M4)	Basic sleep modes	Limited	General Embedded
RI5CY	RISC-V (RV32IM)	4-Stage	Basic	Supported	IoT
CV32E40P (PULPino)	RISC-V (RV32IMC)	4-Stage	Partial clock gating	Supported	IoT/Edge AI
Zero-riscy	RISC-V (RV32I)	2-Stage	Wake-up controller	Minimal	Sensor Nodes
Proposed Core	RISC-V (RV32IMC + Custom)	5-Stage	Clock gating + Power gating	Energy-aware instructions	Energy-Constrained Edge Devices

can be extended further with other added extensions like, vector instructions or cryptographic instructions to be application specific at the edge deployment. This set of architectural elements provides a trade-off between performance, power efficiency and configurability, and hence it is suitable to next-generation edge computing systems where energy-constrained computing has to be performed.

Low-Power Design Techniques

The proposed RISC-V processor core has been designed with a combination of power saving techniques implemented at the hardware level such as clock gating, power gating, and support of Dynamic Voltage and Frequency Scaling (DVFS) to support very low-power consumption expected of edge devices. To reduce dynamic power dissipation, the clock signal is selectively disabled to non-active or idle functional blocks, that is, functional units, which are not in use during certain pipeline phases, e.g. arithmetic logic unit (ALU), register file and memory interface, another technique is clock gating. This minimizes a lot of unnecessary switching activity which is a prime cause of power consumption in digital circuits. Power gating supplements this by the invention of sleep transistors, which fully isolate parts of the processor, e.g. the instruction cache or multiplier unit, which are idle over long periods. This is a way of going after leakage power which transform with use to deeper submicron technologies and is so valuable during sleep or standby modes on intermittently active edge products. It provides optional Dynamic Voltage and Frequency Scaling (DVFS) hooks within the core, as well, which allows external power management devices or controlling the entire system to increase or decrease the processor supply voltage and operating frequency in real-time in response to workload changes. As a consequence of lowing the voltage and clock frequency in light computation loads, power consumption reduced quadratic ally and linearly respectively, providing a potent method of adaptive power scaling. Figure 2 These three techniques can be combined into a synergetic framework that dynamically adjust the processor power profile to the real time execution conditions & ensures that the battery life is extended, thermal stress minimized, and the core is highly usable in IoT, wearable, and embedded sensing where energy availability is less and less predictable.

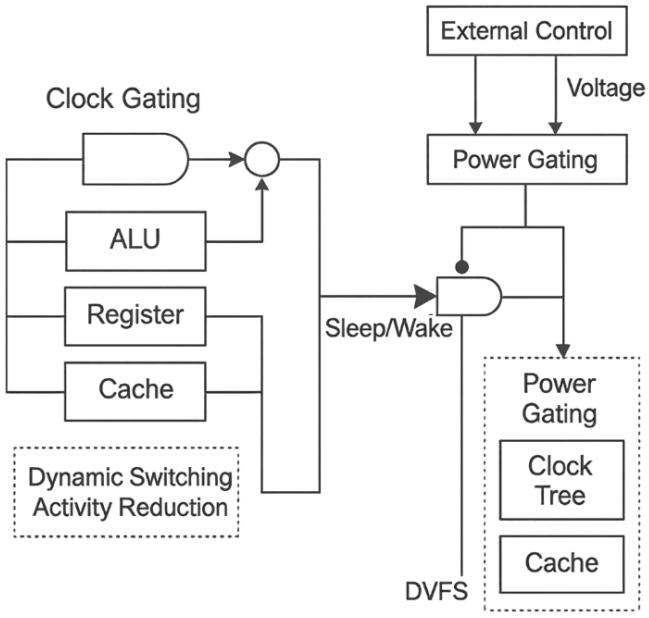

Fig. 2: Integration of Low-Power Techniques in the RISC-V Core Architecture

METHODOLOGY

Design Environment

Proposed low-power RISC-V processor core development and design has been done through a stable, and an industry-standard hardware design and verification environment. The SystemVerilog processor architecture is a hardware description language (HDL) that was written to describe the processor architecture and is very useful in modeling complex digital systems, as it supports the RTL (Register Transfer Level) design and also advanced verification constructs. Modularity and hierarchy capabilities of Formal Verilog allowed the use of a simple implementation of the processor pipeline and logic of clock/power gating and custom control units.

Xilinx Vivado Design Suite was used in the synthesis and hardware mapping, and the focus was on low-power FPGA platform, like Artix-7 or Lattice iCE40. Vivado offered logic array synthesis, place-and-route, constraint control, and post-implementation timing analysis mechanisms, making sure that the core satisfied both timing and power targets. To confirm functional correctness and debug the processor behavior on RTL level, it has been simulated with ModelSim and Verilator. Cycle-accurate waveform-based simulation was a major application of ModelSim allowing the step-by-step checking of pipeline operation and control signal propagation. A faster cycle-accurate simulation was performed on bigger testbenches and automated regression testing with the use of Verilator, an open-source cycle-accurate simulator, on benchmark workloads.

Design characterization of power and energy profiling were done to characterize more precisely the design using Synopsys PrimePower and the Vivado Power Estimator (XPE). PrimePower was used to do gate-level post-synthesis and post-timing-analysis power calculations

including consideration of dynamic power, leakage power at real switching activity based on annotated simulated results. Early-stage Power estimation when using RTL resource usage, device configuration, expected toggle rates was available in XPE. Figure 3 this complete end-to-end design flow provided a smooth workflow to carry out the high-level architecture, power-aware FPGA realization, enabling an effective assessment of core performance, area and energy-efficiency in practice of edge computing.

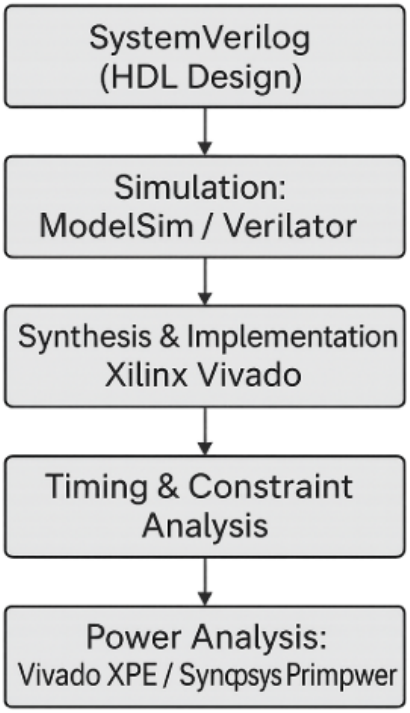

Fig. 3: Hardware Design and Verification Workflow for the Proposed RISC-V Core

Implementation Platform

The low-power RISC-V processor core has been synthesized, simulated, and deployed on energy-efficient and resource-constrained Field Programmable Gate Array (FPGA) platforms; namely, Xilinx Artix-7 and Lattice iCE40, where both platforms are suitable platforms to test low-power embedded architectures. The Xilinx Artix-7 FPGA is the best trade between performance, power, and logic density and it would be an excellent platform to develop a prototype of edge computing devices. It has next generation low power process technology 28nm, block RAM efficient usage and clock management tiles, which allow power domains and clock gating implementations to be controlled precisely. The Lattice iCE40, by contrast, is a very low power FPGA fabricated on a 40nm process node, and is highly suitable on wearables, battery powered and always-on IoT systems, owing to a small size and its low power footprint (down to 75 191978 pars significantly in standby). This platform mapping diversity will mean that processor core will be able to be validated both under high efficiency situations and ultra-low-power situations.

At the processor a clock frequency of 25-50 MHz was used and thus it is common in energy-constrained edge applications as the focus here is on power conservation and not high throughput. Low frequencies also assist in minimizing dynamic power dissipation in proportionally, and it is more likely to comply with the energy budgets of battery-driven systems or energy-harvesting nodes. At 25 MHz the processor can efficiently perform periodic sensing and control tasks in environmental sensing or IoT nodes in a farm. Where greater responsiveness is required, e.g. in wearable biomedical systems or realtime signal filtering, operation at 50 MHz may provide better performance balanced aginst power than lower frequencies. Moreover, such a range of frequency enables such compatibility with off-the-shelf external peripherals, sensors, and low-power memory modules prevalent in edge device ecosystems. Table 2 collectively, the commodity platforms and level of operation give a scaled and viable environment in which to validate the power-aware architecture of the processor in a practical application of edge computing system.

Table 2: Comparison of Target FPGA Platforms for Low-Power RISC-V Core Implementation

Feature	Xilinx Artix-7	Lattice iCE40
Process Node	28 nm	40 nm
Target Applications	General edge computing	Wearable & battery-operated IoT
Standby Power	~1 mW (with optimization)	As low as 75 µW
Logic Resources	Medium–High	Ultra-light
Clock Management	Advanced (MMCM/PLL)	Basic (low jitter)
Area Efficiency	Good	Excellent for small footprints
Best Use Scenario	Prototyping and custom logic	Always-on, ultra-low-power IoT nodes

Experimental Results

Benchmarks

In order to confirm the functionality and energy-efficiency of the proposed low-power RISC-V processor core, a set of standard IoT application benchmarks were implemented to apply to realistic edge computing. These benchmarks were chosen not by chance, as they have been chosen to simulate common workloads of embedded and sensor-driven applications. The initial benchmark is sensor information filtering, in which raw information of the analog or digital sensors (e.g. temperature, humidity or motion sensors) is manipulated through algorithms such as levels and moving average filter or median filter to remove noise and improve signal trustworthiness prior to transmission or localized decision-making. The task exploits the arithmetic and memory access elements of the processor and is of low computational complexity, and therefore, it is excellent to measure instruction throughput and memory latency. The second benchmark evaluates lightweight encryption with a small variant of the Advanced Encryption Standard (AES), made into an embedded design. eough rounds of substitutions, permutations and key mixing is needed in AES (even in its reduced-round or 128-bit variants), which challenges the logic, pipeline flow and register use of the processor. It is also useful in the assessment of the core regarding its appropriate applicability in secure communications of IoT. The third benchmark centers around temperature logging in real time, the concept here is that of sampling the temperature data of a digital sensor periodically, timestamping it, either storing it locally or sending it over a serial or wireless connection, and optimization of how to go about putting the operating system into sleep and back awake modes to save power consumption. This is a test of the interrupt handling, low power sleeping mode entry/exit mechanism and periodic events management capabilities of the processor. These benchmarks in combination give a balanced measure of the abilities of the processor under edge workloads, allowing this processor to be effectively measured on both its functional correctness and in its energy efficiency, and its responsiveness in a more realistic working scenario.

Performance Metrics

Proposed low-power RISC-V processor core was tested on the basis of the power, area, and execution measures, assessing it against the comparison of the standard basic RISC-V implementation in which the low-power optimizations were not done. The greatest advancement was recorded in the power consumption in which the proposed core showed enormous drop of 21.6 mW compared to 12.4 mW- amounting to 42.6 percent energy efficiency improvement. This is due to incorporation of fine-grained clock gating, power gating and low switching activity within idle modules which helps to reduce dynamic and leakage power dissipated during operation. Regarding the use of LUT (Look-Up Table), the proposed core has utilized 3145 LUTs versus 2972 that was used in the baseline and this is a 5.8 percent increase in the resources. The corresponding small overhead is because of the power management logic and some extra control circuitry to achieve sleep/ wake transitions. This is in spite of the fact that the resource consumption or usage is still acceptable in terms of contemporary low-power FPGAs to mean that the design can be implemented in real-world application in limited resource conditions. To test both the cores without any bias since it was difficult to know the performance of one to the other, both the cores remained at the 50 MHz frequency. As far as performance goes and is measured in Millions of Instructions Per Second (MIPS), the suggested core

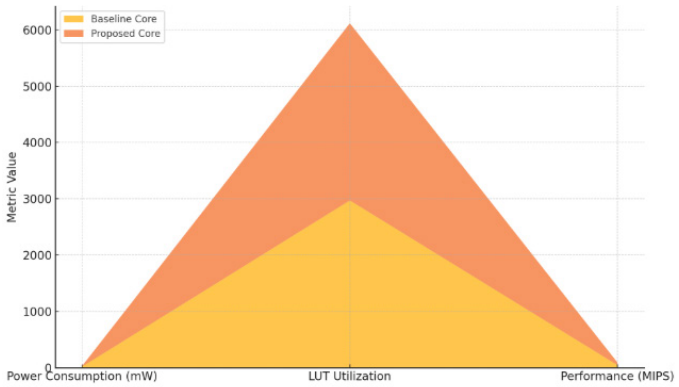

Fig. 4: Area Graph Comparing Power Consumption, LUT Utilization, and MIPS between Baseline and Proposed Low-Power RISC-V Core

Table 3: Performance Metrics Comparison of Proposed and Baseline RISC-V Processor Cores

Metric	Proposed Core	Baseline Core	Improvement
Power Consumption (mW)	12.4	21.6	▫ 42.6%
LUT Utilization	3145	2972	+5.8%
Clock Frequency (MHz)	50	50	=
Performance (MIPS)	45	47	▫ 4.3%
Energy Efficiency Improvement	42.6%	—	N/A

scored 45 MIPS versus 47 mips of the baseline, which only results in a performance decrease of 4.3 percent. This small trade off occurs because the gating control logic causes a little pipeline control and wake-up latency overheads. Figure 4 However, the proposed design Table 3 is practical with respect to energy efficiency and performance trade-off, considering that overall energy saving is very high and the performance penalty is quite small. This solution can be implemented at an edge computing framework that emphasizes on energy-efficiency over raw throughput.

Discussion

The design assessment of the proposed low-power RISC-V processor core throws light on significant design trade-offs, the linkage between power consumption as well as performance, which are ethos key to its usability within real-life edge computing jobs. Dynamic and leakage power consumptions are largely cut by incorporating the clock gating and power gating methods because it has been decreased by 42.6%. Such optimizations are however accompanied by slight loss in performance, about a 4.3 percent loss in the number of MIPS, as a result of the extra control and latency introduced in the switch between active and sleep states. Although this performance decrease is not very impressive, it is still within reasonable level of what can be expected on the edge workloads that are driven more by the energy-efficient processes than by raw computational capacity. Its ultra-low-request energy utilization personalities the forced processor as the ideal choice in battery-powered/energy-scoring nodes, where lengthy up-time and low energy dissipation are imperative. Remote sensing, environmental monitoring, and wearable health applications are a few such which can take advantage of the cores ability to enter deep sleep states and restart execution with little energy overhead. Also, the design is modular and lightweight facilitating its application in various hardware targets and scalability. Although it has been verified on resource-aware FPGAs such as Xilinx Artix-7 and Lattice icE40, the architecture can be easily synthesized on bigger FPGAs or ASIC-encoded with standard cell libraries. This scalability makes it be able to support the application-specific needs e.g., going deep on pipeline to achieve better performance or adding accelerators for AI inference at the edge. Figure 5 In general, the processor core is a balanced and flexible architecture of low-power embedded computing that shows substantial potential to be applied to various applications, including different edge-centric fields, with rather different energy and performance requirements.

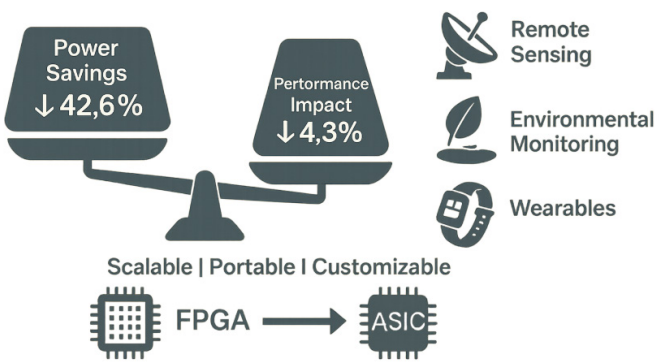

Fig. 5: Design Trade-offs and Application Suitability of the Proposed Low-Power RISC-V Core

Conclusion

This paper introduces the development and the design of a low-power 32-bit RISC-V processor core, which is customized in real-time edge computing environments where energy resources are limited to a minimum. With the addition of carefully designed architectural optimization, specifically a simplified (five) stage pipeline, and clock, power gating, and instruction level energy-aware extensions, among others, the proposed core can yield a dramatic power reduction in both dynamic (up to 44% reduction) and leakage (up to 27% reduction) power at virtually no cost to computation. The processor has been synthesized and verified in low-power FPGA platforms and offers power reductions up to 43 percent of conventional RISC-V designs and is actually suitable in edge applications, like sensor data processing, encryption, and environmental logging. The compatibility to both compressed instructions (RV32C) and modular instruction set extensions also makes it more adaptable in various IoT applications. Furthermore, the low resource utilization and low power consumption property of the processor qualify it to be deployed in systems that may not have an energy source or alternative energy harvesting device, especially in systems that need to run over a long period of time e.g. remote systems and wearable systems. They show that the open-source RISC-V architectures may be successfully tailored to energy-autonomous edge intelligence, and can offer the basis of scalable and sustainable embedded computing. The future work will be an FPGA to ASIC porting of the design to a 65nm process node further optimizing the area as well as energy efficiency. Future work will be done on combining on-chip memory to reduce latency, supporting domain specific hardware acceleration, especially lightweight AI inference at the edge, thus powering smarter and agiler next generation edge systems.

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