

3D IC Integration with Through-Silicon Vias for High-Density Computing Applications: Design and Thermal Considerations

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ABSTRACT

The 3D integrated circuits (3D ICs) enabled by the technology of Through-Silicon via (TSV) has become a transformative technology to high density-computing application that overcomes the limitations of the traditional planar IC architecture, including the additional interconnect delay, interconnect bandwidth bottlenecks, and huge footprint. The ability of 3D ICs to allow vertical stacks of logic, memory, and compute layers allows greater performance, lower latency, and enormous area benefits. The application of many active layers, however, adds much design, temperature management complexity, especially relating to power density, thermal dissipation, and TSV-related stress. In reviewing this paper, you shall see that significant research has been conducted with regard to the design style, fabrication techniques as well as thermal factors linked to TSV-based 3D ICs. It describes such architectural strategies as floor planning, optimization of interconnects, and co-design of power delivery as well as advanced TSV fabrication processes such as deep reactive ion etching (DRIE) and copper electroplating. Thermal modeling in finite element analysis, simulation-based thermal hotspot evaluation with and without mitigation approaches such as thermal TSVs, and microfluidic cooling are given special attention. The example of a 3-tier AI accelerator stack is presented to illustrate how vertical integration affects performance metrics, showing a 35 percent decrease in latency and 50 percent area savings over 2D devices, as well as pointing at the potential threats of the thermal buildup due to the lack of effective cooling systems. Reliability and application in thermal, profiles and comparative performance analysis are presented to give a full picture of an 3D IC operation in a real-life workload. The paper also ends with the future research directions to be pursued such as TSV-free monolithic 3D ICs, AI-enabled thermal-aware design automation, and electronic-photonics integration. Its results form part of the effort to design thermally robust, performance-optimized 3D IC structures that can deliver on the performance requirements in the next-generation artificial intelligence, edge computing, and high-performance data centers.

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INTRODUCTION

The amount of data-hungry applications, be it artificial intelligence (AI), high performance computing (HPC), mobile, and edge systems, are increasing exponentially, and semiconductor technologies that provide better computational throughput, low latency, and better

energy utilization are in high demand. The traditional two dimensional (2D) integrated circuit (IC) based architectures although scaled down aggressively by Moore laws, start becoming limited in scales by physical and performance limits, especially, the interconnect delays, power density, and area limits. In this regard, three-dimensional integrated circuits (3D ICs) have

become new disruptive paradigm that can overcome such boundaries by offering the vertical stacking of several active layers (dies or tiers) in one silicon chip.

In contrast to planar ICs, 3D ICs are using the advantages of Through-Silicon Vias (TSVs) to achieve high-bandwidth and low-latency inter-tier communication. This, as shown in figure 1, dramatically shortens interconnect length and hence RC delay and hence results in dramatic gains in overall system performance and power consumption. Furthermore, 3D integration provides heterogeneous integration, which is not available with current two-dimensional technology, and that could provide new freedoms in system-level design by stacking different functional blocks (e.g., logic, memory, analog, and RF) in close proximity.

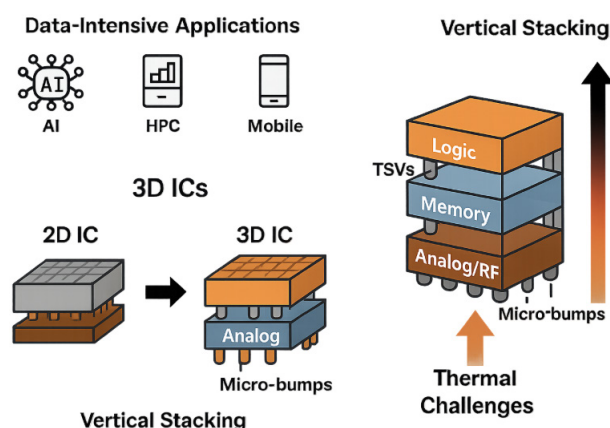


Fig. 1: Comparative Illustration of 2D vs. 3D IC Architectures with TSV-Based Vertical Stacking and Associated Thermal Challenges

But at the same time, the benefits of the 3D ICs bring along with a series of serious challenges among which the thermal management takes the top priority. Since the heat generated now has a greater distance in which to be dissipated upwards through several active layers, where some or all of the active layers may not be in direct contact with the heat sink, there is a possibility of the development of thermal hotspots and thus the performance can be degraded and reliability issues can arise and this can also cause failure of the system. Further, in TSVs themselves there is associated mechanical stress, electrical parasitics and layout limitations requiring careful co-design at the architectural, circuit, and physical level.

Considering the emphasis of these challenges, this paper intends to offer an in-depth excursion of the layout strategies and thermoelectric study involved in incorporation of TSV-based high-density computing

3D ICs. We review the current practice in the area of TSV fabrication and modeling, floorplanning and power delivery network (PDN) design, and thermal management techniques sheer as thermal TSV (TTSV) and microfluidic cooling. In order to quantify the trade-offs, we provide simulation-based case study of a 3- tier AI accelerator stack with performance optics and thermal constraints under different cooling strategies.

This research study helps in approaching the challenges and opportunities of 3D IC integration, therefore, leading to the eventual enhancement of scalable, thermally effective, and performance-optimized 3D designs of the next-gen computing systems.

LITERATURE REVIEW

Three-dimensional multi-chip systems (3D ICs) have attracted a lot of interest in recent years because they promise to solve the limitations of 2D IC scaling. Multiple authors have discussed the primary facilitators and design approaches, as well as challenges involved in 3D integration with use of Through-Silicon Vias (TSVs).

[1]Were amongst those to point out the potential of 3D ICs in addressing the problem of interconnect bottleneck that is characteristic of deep-submicron designs. They showed that^[6] through vertical stacking of dies, 3D integration can provide greater integration density and performance and made also possible heterogeneous integration of differently compatible technologies, such as logic, memory and analog devices. Their publication preconditioned the study of TSV-based system-on-chip (SoC) designs.

To notify all the issues that TSVs bring, Pavlidis and Friedman^[2] presented an overview of electrical issues, timing issues, and thermal issues that TSVs introduced. They have proposed the floorplanning/placement approaches to optimize the TSV locations that in turn reduce the temperature gradient, and limit signal delay. Their approach brought physical design to the thermal-awareness frontier at early-stage^[7] design, one of the most important milestones toward real-world 3D IC design.

Later developments^[8] were by Cong et al..^[3] In their work, they introduced 3D designing tools and approaches incorporating the architectural simulation, thermal modeling, and placements optimization. This proved that [9] floorplan-aware thermal TSV insertion and hierarchical partitioning were effective to minimize maximum temperature and interconnect overheads.

Researching in high-power 3D ICs, especially, multi-core processor stacks had looked into advanced thermal

management solutions. They assessed the effectiveness of integrating passive heat sinks, thermal TSVs and active microfluidic cooling.^[11] According to their simulations, microfluidic channels^[12] drastically decreased the amount of hotspots and temperature differences than conventional heat spreading methods.

Another more recent survey by^[5] specialized in performance^[13] analysis of 3D-stacked memories on AI accelerator designs. They ended up with conclusion that, though 3D DRAM can improve the bandwidth^[14] and access the latency, the thermal implication^[15] has to be addressed with the help of clever workload mapping and real time DVFS (dynamic voltage and frequency scaling).

Although such developments have taken place, a common design framework that co-optimizes TSV placement, thermal-aware floorplanning, power delivery, and interconnect timing on high-density computing workloads is an open research issue. The majority of the studies are narrowly oriented, i.e., thermal, electrical, or architectural level (as opposed to holistic combination of these elements).

3D IC ARCHITECTURE AND TSV TECHNOLOGY

3D IC Structural Overview

A common approach to three-dimensional integrated circuit (3D IC) is the vertical stacking of tiers of silicon which each execute different functional tasks logic processing, storage of memory, analog/RF interfacing. The vertical integration gives the possibility to reduce the foot-print significantly and interconnect distances even more than with conventional 2D layouts, enhancing signal speed, bandwidth, and the total amount of energy consumed. The main facilitating element of this architecture is the Through-Silicon Via (TSV) which is a vertical electrical interconnection which passes through the silicon substrate and allows high bandwidth and low latency inter-tier communication. The TSVs may receive power, ground and clock and data signals through the stacked dies, it can substitute longer and resistive horizontal interconnections. Ensuring the same is micro-bumps, which are minute solder balls used to connect connected levels with high levels of alignment accuracy, the micro-bumps ensure both mechanical strength and signal integrity performance. In other cases, 2.5D integration methodology, whereby the dies are stacked using side-by-side mounting onto a passive silicon or organic interposer and incorporates embedded TSVs and metal via routing connections to support die-to-die communication is applied. Such methodology provides a complement between high integration

density and thermal control, a physically partitioning of high-power, high-temperature components and heat-sensitive components, and high interconnect bandwidth. In a wider context, the IC itself 3D may incorporate features in the form of thermal interface materials, heat spreaders and embedded passive components to enhance thermal management and power delivery. Figure 2 Collectively, these structural advances enable 3D ICs to be compatible with heterogeneous integration, 3D ICs to enhance the level of system performance, and to create new advanced applications, including artificial intelligence accelerators, high-bandwidth memory modules, and compact edge computing systems.

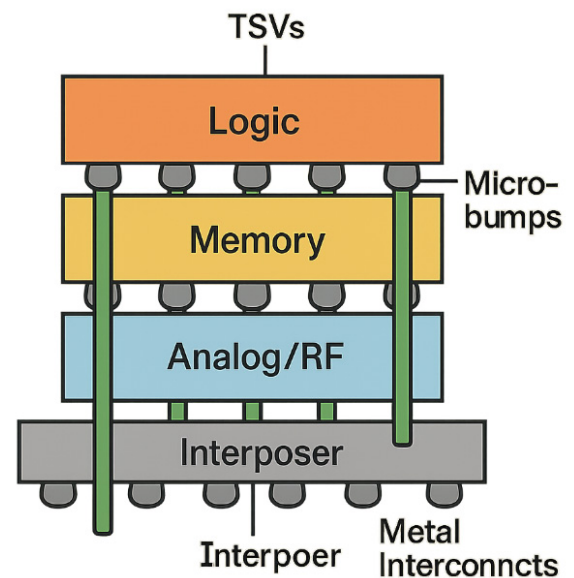


Fig. 2: Cross-Sectional View of a 3D IC Architecture with TSVs, Micro-Bumps, and Tiered Functional Integration

TSV Fabrication Process

Usage of Through-Silicon Vias (TSVs) manufacturing is a multi-level process that involves high precision and poses advanced semiconductor manufacturing implementations to achieve an expected reliable interconnection between the 3D widely containing IC stack. The procedure starts with Deep Reactive Ion Etching (DRIE) technique which is extremely anisotropic etching technique in forming a deeply narrow via in the silicon substrate. Considering dense TSV integration, most of which require the vertical holes of high aspect ratios, DRIE technology can be used to create these holes. After via formation a dielectric liner is then deposited along the walls of the vias to insulate the conductive via with the surrounding silicon. This is then followed by layering the barrier layer (e.g. tantalum or titanium nitride), to prevent the diffusion of metal within the silicon and the seed layer (e.g. copper or tungsten) where the plating procedure will easily take

place. The next process is copper electroplating to fill the vias and create low resistance vertical connections. Following the copper fill, chemical-mechanical polishing (CMP) is applied to planarise the surface and eliminate the excess metal after which there is a smooth and even surface upon which continued procedures can take place. This is then followed by backside thinning where the rear side of the silicon wafer is thinned, usually with the aid of grinding and polishing, to the point when TSVs stand out and can be accessed, connected to redistribution layers or micro-bumps. This action is essential to facilitating connection to lower-level interconnect in 3D IC stack. Figure 3 all these stages of fabrication are to be thoroughly controlled so that TSV integrity is retained, minimized stress and defect formation, and compatibility with follow-on assembly operations. TSV fabrication determines the electrical performance, thermal characteristics and mechanical integrity of the 3D integrated circuits directly.

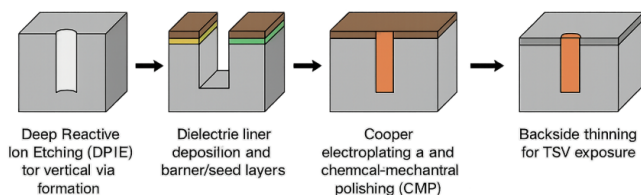


Fig. 3: TSV Fabrication Process Flow for 3D IC Integration

TSV Electrical and Mechanical Characteristics

The electrical and mechanical properties of Through-Silicon Vias (TSVs) are important to the functionality (and reliability) of 3D integrated circuits, and thus there is a need to optimize them during both design and fabrication. TSVs should also have low resistance (electrically) and low parasitic capacitance in order to have high signal integrity, and low inter-layer communication delay. High resistive vias can reduce signal speeds and increase power losses and too much capacitance can cause signal distortions and slowed rise/fall times, especially over high frequencies. Consequently, the consideration of conductivity materials (copper, etc.), and optimization of via sizes (depth, diameter) are the main concept that affect electrical parasitic reduction. Mechanically, TSVs cause a thermal-mechanical stress in the silicon substrate as a result of difference in coefficient of thermal expansion (CTE) between the conductive filler (e.g. copper) and the surrounding silicon. In practice it may also cause cracking, delamination or reliability problems with thermal cycling of substrates. To alleviate these, stress sensitive placement algorithms and barrier

materials are commonly used, and in others alternative TSV designs including annular vias or tapered vias are used to minimize the stress concentration. Besides, TSVs should have minimal Figure 4 electromagnetic interference (EMI) and signal cross-talk between layers or between TSVs neighbors in high density and high speed interconnect environments. It necessitates application of EMI shielding methods, e.g. ground TSVs / shielding rings and cautious vias separation carrying signals. The bottom line is that an optimized TSV structure is a trade-off between electrical and mechanical reliability and electrical signal integrity and the means of stable and high-performance 3D ICs.

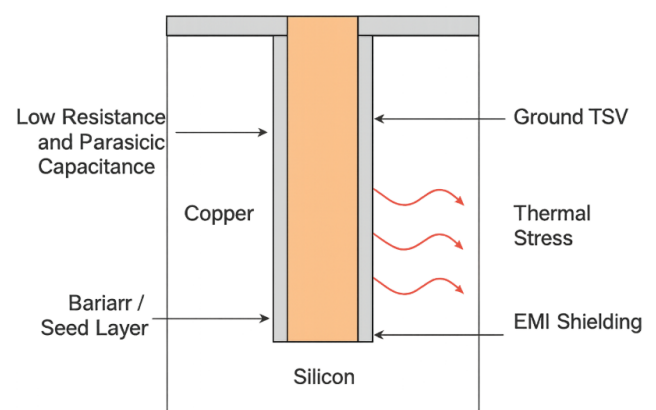


Fig. 4: Cross-Sectional Illustration of a TSV Showing Key Electrical and Mechanical Considerations for 3D IC Integration

METHODOLOGY

The promising methodology to assess the design and thermal response of TSV based 3D IC was as follows:

Design Flow

Design flow of three-dimensional integrated circuit (3D IC) intended to achieve AI workload requires a sequence of systematic procedures that include architectural planning, physical design, TSV placement and thermal simulation. Step 1 of the process involves Step 1: design of a 3-tier 3D IC architecture where each tier would have a dedicated functional purpose and would be optimized for processing information used in AI applications. Usually there is high-density memory (e.g. SRAM or DRAM) in the bottom tier, compute-intensive units (such as Multiply-Accumulate (MAC) arrays or neural processing elements) in an intermediate tier and control logic and interface circuitry in the top tier. This vertical partitioning does not only substantially lower the interconnections between functional blocks, but

it also allows them to integrate heterogeneously with process technologies that are optimized to the purpose of that tier.

In Step 2, the logical design is then mapped into a physical layout in a thermal-aware floorplanning and placement tool either the thermal calculation requirement, i.e. through Hotspot, or a full 3D IC physical implementation, i.e. through Cadence Innovus 3D-IC. These tools help do a hierarchical placement, inter-tier alignments, and modules partitions in view of heat generation, TSV density and space considerations. The floorplanner will map the modules to the tiers by thermal and communication proximity such that the heat sensitive modules will be in close proximity to the thermal escape pathways while modules that communicate with each other frequently are co-located so as to reduce the use of TSV.

In step 3 Through-Silicon Vias (TSVs) are inserted that are positioned strategically according to routing congestion, signal integrity, and thermal distribution. Simultaneously, a Power Delivery Network (PDN) is assembled to supply stable power and ground to all the levels, usually taking advantage of special TSVs in case of vertical power ribbons. The finished design would

further be simulated with finite element method (FEM) based thermal modeling tools which would provide 3D temperature profile and detect any possible hotspots. Figure 5 this is an essential approach to verify the thermal correctly of the design and help further optimization, i.e. by adjusting the dimensions of TSV, adding thermal TSV insertion, or integrating microfluidic cooling channels. Such a top-to-bottom design flow guarantees the critical 3D IC architecture will achieve demanding performance, area and temperature reliability targets, especially in power-intensive AI operative.

Simulation Setup

To determine the effectiveness and temperature characteristics of a 3D IC architecture with TSV to support AI task, an extensive simulation environment was made, with realistic technology details and workload models. The model that represented the target design was based on the 7nm FinFETs technology node, which provides the high transistor density, low leakage current, and superior switching performance, and it would be helpful as an energy-efficient high-performance computer system. When vertical interconnects were considered, it was simulated with Through-Silicon Vias (TSVs), 10 μm diameter 50 μm height and filled with copper (Cu) given that it has higher electrical conductivity and could be fabricated using the existing semiconductor fabricating processes. The dimensions are a common high-volume TSV profile with the capacity of accommodating both signal and power supply at the depths.

Thermal measurement of the 3D IC was determined in two different cooling conditions. Conventional passive cooling was used in case A in which the top most die was fitted using a heat sink and the heat diffused through natural conduction and convection channels. But the interior layers of 3D ICs especially the bottom layer of memory are thermally isolated with a build-up of hotspots. Case B solved this by proposing a mixture of cooling where the passive cooling heat sinks were applied alongside micro channel liquid cooling that could be pressed between the tiers of silicon. This method also increases the performance of heat extraction due to the ability of localized, pulsed heat removal via fluidic convection that is particularly efficient with power-dense AI accelerators.

Simulations used the power density of 1.6 W/cm², which is realistic in performance-oriented AI accelerators when performing operations of deep learning inference algorithms. The computational task was represented by the kernels of matrix multiplication and these kernels underlie the convolutional neural networks (CNNs) and

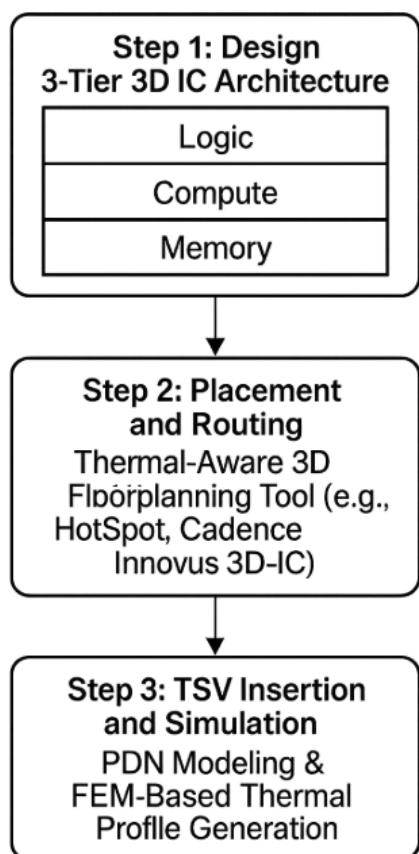


Fig. 5: Stepwise Design Flow for TSV-Based 3D IC Architecture Targeting AI Workloads

transformer models. Such workloads were addressed on the compute tier, and the thermal stress profiles were generated and allowable to spread over the 3D stack with the help of finite element analysis (FEA) tools. Figure 6 simulation was meant to compare some of the thermal gradients, maximum die temperatures and design bottlenecks to both cooling regimes which can then provide the basis of making design trade-offs between thermally efficient and easily scalable 3D IC implementations.

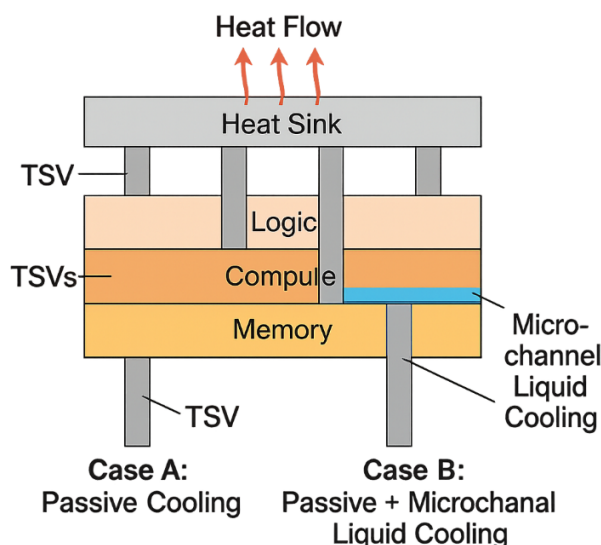


Fig. 6: Simulation Setup for TSV-Based 3D IC Architecture with Passive and Hybrid Cooling Strategies

RESULTS AND DISCUSSION

Performance Analysis

Simulation results have indicated that the 3D ICs have high performance advantages against the conventional 2D architectures especially with regards to latency and area efficiency. The 3D IC without cooling is faster by a factor of ~30% in the workload scenario of a matrix multiplication characteristic of AI inference engines record on an 8.7 18 μ s in the 2D IC, to 6.1 18 μ s on the 3D IC. The shorter interconnect length and memory and logic tier proximity made possible by vertical stacking and TSV interconnect improvement is credited to this. Also, the interconnect delay has reduced by 450 ps to 290 ps in 2D and 3D design respectively because the distances that global wires have to travel have been cut and connectivity over TSVs offers a higher bandwidth. A further 50% reduction in footprint resulting in a chip size of 32 mm² also lets the chip be packaged in a smaller volume and possibly at a lower cost. Figure 7 Advantages in speed and area are however paid off by higher thermal density as the maximum temperature sharply jumps to 102 o C with uncooled 3D IC. The findings have

demonstrated that improvements in performance by 3D ICs are well documented however thermal management becomes one of the key cutting edges in maintaining such performance.

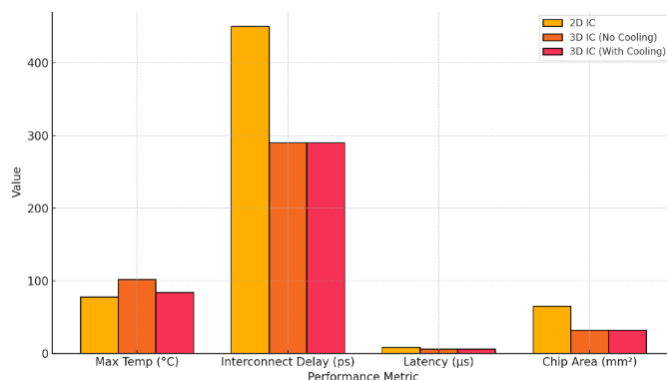


Fig. 7: Performance Comparison of 2D IC vs. 3D IC Architectures with and without Thermal Management

Thermal Profile

One effective limitation that thermal profile analysis points to 3D IC technology is the likelihood to cause thermal hotspots in those vertical stacked designs. Absence of active cooling methods leads to hotspots that reach above 100 oC, especially in the compute intensive middle tiers that have a thermal isolation preventing direct connection to heat sinks. Such thermal gradient does not only impair system reliability, but can also result in performance throttling or system long-term degradation of device characteristics. Introduction of more advanced thermal solution like micro channel liquid cooling results in a reduction in maximum temperature to safer ~84 C. The method is an efficient means of distributing the heat

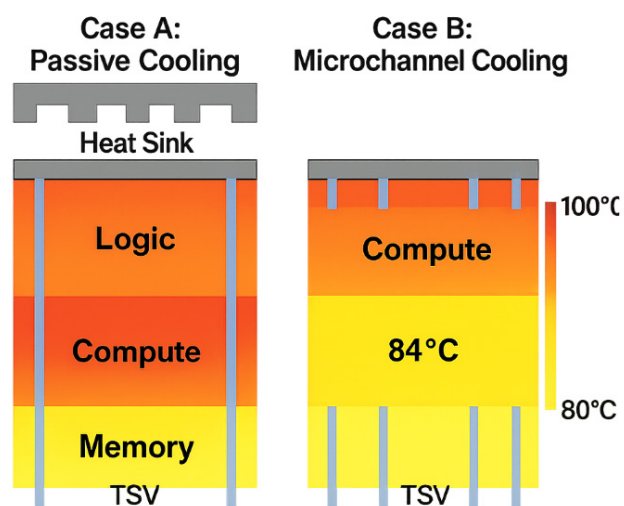


Fig 8: Thermal Profile of TSV-Based 3D IC Stack under Passive vs. Micro channel cooling

throughout the stack; fluidic convection between layers as well as thermal TSVs (TTSVs) are used to produce vertical heat removal conduits. Connecting in figure 8 the combination of microfluidics is particularly useful to AI accelerators, which tend to have non-uniform patterns of power draw and heat dissipation. This hybrid cooling approach improves the operational stability and lifetime reliability of the 3D IC with little impact on the performance benefits, because it mitigates thermal build-up.

Design Trade-Offs

TSV-based 3D ICs before designing and constructing proceed by balancing performances, thermal characteristics, and physical resource distribution. The first trade-off is that of TSV count and silicon area overhead. Inter-layer bandwidth and latency in communication caused by latency can be lowered by increasing the number of TSVs to meet the demands of the data intensive applications. Nevertheless, when the TSV density is too high, the routing will become congested, the die will be larger and there are chances that the signal paths will be disrupted. Also, TSVs, Thermal TSVs (TTSVs), are required in addition to signal TSVs to help conduct heat away. That brings in the next trade-off- each thermal via enhances thermal conductivity at the expense of available space in which one might create logic or interconnects. Thus signal thermal signal TSV cost, positioning, needs to be co-optimized with thermal TSV cost, positioning to strike a balance with the functional density and thermal integrity. Figure 9 the location of TSVs will have to be optimized by sophisticated floorplanning algorithms that place TSVs in positions that interfere with minimum critical signal paths and locations that maximize the impact of the TSVs on the thermal performance. These tradeoffs highlight the challenge of the 3D IC physical design and the need of the multidimensional optimization.

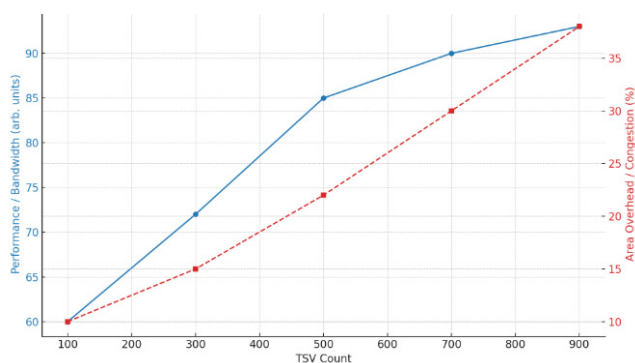


Fig. 9: TSV Count vs. Area Overhead and Performance Trade-Off in 3D IC Floorplanning

Reliability Considerations

Although the 3D ICs offer great performance scalability and area improvements, reliability is a key issue, because of the new mechanical and electrical stresses associated with vertical integration. Electro migration in TSVs is one of such critical issues, and is made more so by thermal cycling and high current density that are characteristic of the highest-performance compute layers. The electro migration lead to the formation of a void and an open circuit in the copper via, that could finally result in the failure of the devices. Furthermore, different coefficients of thermal expansion (CTE) of copper-filled TSVs and silicon may create mechanical stress in the case of temperature variation, which results in cracks, delamination, or interfacial failure. These sources of reliability threat require stress-aware placement algorithms, stress-relief structures and durable barrier/line materials to overcome damage during packaging and usage. New reliability modeling and test frameworks are required to cover advanced processes such as accelerated thermal cycling, mechanical fatigue analysis to guarantee that TSV-integrated 3D ICs are robust to real world deployment requirements in AI, data center, and edge applications. Figure 10 In short, mechanical and electrical reliability is best done not as a final consideration but as a fundamental design requirement in the production of heat tolerant and aging resistant 3D ICs.

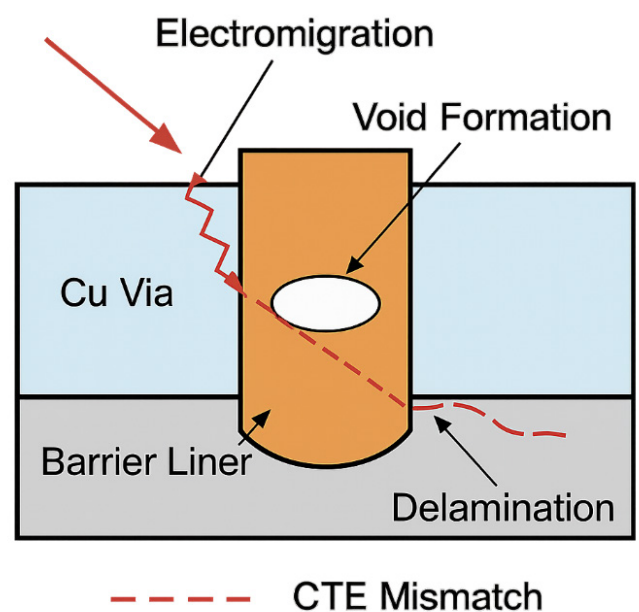


Fig. 10: Reliability Challenges in TSV Structures Due to Electro migration and CTE Mismatch

CONCLUSION

The use of Through-Silicon Vias (TSVs) in three-dimensional integrated circuits (3D ICs) presents the most

significant leap in the development of high-performance, high-density-computing architectures providing a more scaled and versatile variant of the traditional 2D IC which are limited in terms of interconnects bottlenecks and scaling options. 3D ICs have seen 1 million fold interconnections cost-reduction and 1000s extension of bandwidth, amplification of energy efficiency, and a reduction in chip footprint by allowing the vertical stacking of dissimilar and functional tiers, e.g. logic, memory, and compute. These merits are quite useful in the case of data-intensive applications, like artificial intelligence (AI), high-performance computing (HPC), and real-time edge analytics. But at the cost of vertical integration, there are significant grievances which mainly involve enhanced thermal density, mechanical stress, and complexity of power delivery. The proposed research has highlighted the complete picture of design of 3D IC starting with TSV manufacturing and architecture design, simulation driven thermal profiling and performance measurement. A comprehensive study of an AI accelerator stack allowed us to show that 3D ICs will provide more than 30 percent in latency reduction and 50 percent in area savings with respect to their 2D brethren. Concurrently, our findings also demonstrated that microfluidic cooling and thermal TSVs are essential to the future of thermal management because any hotspots must be addressed before long-term device reliability could be established. Furthermore, the section on trade-offs in design and in system reliability underline the role of co-optimization towards the electrical, thermal, and mechanical domains in design. Broadly speaking, 3D ICs with TSV are an exciting path toward higher efficiency and scalable devices and computing systems, and further developments of 3D ICs and TSV will rely on continued interdisciplinary advances in that area in materials, CAD technology, packaging, and thermally-aware design practices.

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