

A Scalable Parallel Processing Architecture for Real-Time and Energy-Efficient Biomedical Signal Analysis in Edge-Enabled Health Monitoring Systems

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ABSTRACT

The trend in wearable Biomedical devices that integrate continuous health monitoring capabilities has also necessitated the need to analyze the wide range of signals in real-time with energy-efficient analysis at the edge. High latency and the lack of scalability require new line-based processing architectures that are more appropriate to perform the real-time computation of electrocardiogram (ECG), electroencephalogram (EEG), and electromyogram (EMG) signals processing. This paper presents a scalable work detector which is tailored towards edge enabled health monitoring systems and which has the goal of parallel processor architecture. The architecture incorporates the modular pipeline architecture and a hardware/software co-design approach such that preprocessing, feature extraction, and classes can be done simultaneously. Versatile balancing of work load across the numerous processing elements promises optimal performance and utilization of energy. It is prototyped on an FPGA based platform with embedded ARM cores and custom accelerators, and it is demonstrated based on real data in the biomedical applications. Results of experimentation show a 65% depletion of the processing latency and 48% enhanced energy efficiency as compared to single-core systems. These results indicate that the proposed architecture can serve as an efficient and scalable architectural solution that can help to realize real-time biomedical signals analysis in future edge-AI healthcare equipment.

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INTRODUCTION

The wearable and implantable biomedical devices are growing faster, and the advancement has transformed the healthcare industry by offering the potential to continuously monitor physiological parameters like electrocardiogram (ECG), electroencephalogram (EEG), and electromyogram (EMG). These systems have been very useful in relation to remote diagnostics, management of chronic illnesses and in real time detection of emergencies. But the overall usefulness of such health monitoring systems depends on their capability to perform biomedical signal processing in real-time with high accuracy, and low latency, and ones that are energy-efficient so that they can be functional over a long period of time on resource-limited platforms.

Broadly speaking, biomedical signal analysis has been carried out either on server or cloud based systems. Although these systems can offer adequate computational power, the communication latency is usually quite high, the power used by these systems due to data transmission, and the privacy of confidential health data is affected. Such shortcomings have motivated the move towards the edge computing paradigms, where the processing occurs on wearable devices or near-edge. Some of the advantages of edge enabled processing include low latency, increased data security and real time reactions. Nonetheless, it is not easy to have complex biomedical signal processing algorithms run on an embedded system, and there are related issues of throughput, and parallelism and power efficiency.

These challenges have been resolved in a number of existing architectures, using both digital signal processors (DSPs), graphics processing units (GPUs) and field-programmable gate arrays (FPGAs). As an example, DSP based systems can only perform adequately when it comes to filtering and transformations since they usually lack parallel processing which is required to perform instantaneous multi-channel analysis. GPU-accelerated methods provide very high throughput, however, being too power consuming to be used on wearable edge devices. FPGA implementation represents an opportunity as an intermediate between parallelizing synthesized pipes and high-performance energy-conservative calculation. Most of the current FPGA-based systems are single purpose and do not scale to support different types of biomedical signals or number of workloads.

Similar to the recent literature, other work like Kim et al.^[1] is more application-specific and limited in generalizability as it proposes a low-power VLSI architecture to detect the ECG signal. Arguably, other attempts by Saponara et al.^[2] examine wearable processing unit employing microcontrollers, yet confront the problem of scalability under multi-modal data streams.

Moreover, edge systems that are augmented with AI, like those discussed in Wang et al.^[3] acknowledge lower latency in place of accuracy because of deep learning inference overhead. The above studies all pin-point the importance of a scalable, modifiable, and energy-efficient parallel processing architecture, which is specially designed to suit edge-enabled biomedical environments and real-time biomedical signal analysis.

A parallel processing architecture that will overcome these drawbacks is proposed in this paper: it is modular and can be scalable; it implements the principles of hardware/software co-design and is dynamic so that optimal performance can be achieved through workload distribution. The proposed architecture, unlike others preceding it, allows configuration of a pipeline of processing elements (PEs) that are optimized to perform heavy-duty signal denoising, feature extraction, and lightweight classification. The architecture is dynamic and dynamically allocatable based on signal type, level of workload and required amount of energy. FPGAs allow a speed-up over the baseline system, with latencies and energy improvements of up to more than three times over the hand-designed single-core baseline implementation up to five times over a DSP-based baseline implementation.

The present proposal will contribute to some major areas to advance real-time biomedical signal analysis, which is supported by the edge-enablement of health

monitoring systems. The first of them is the introduction of a parallel pipeline architecture, scalable to large numbers of streams and designed specifically to process ECG, EEG and EMG signal in real time. This architecture is developed with a hardware/software co-design technique which involves a configurable processing element and a dynamic workload balanced so as to have high performance and flexibility in customisation to different workloads and signal types. The engine is executed on an FPGA platform, making flexible, energy-efficient processing capabilities, responsively in real time. The overall assessment of the architecture on the basis of benchmark biomedical datasets proves the efficiency of the architecture with up to 65% latency reduction in the processing and nearly 48 percent better energy utilization than both the single-core and DSP-based systems. In sum, this paper provides a solid platform of energy-efficient, scaled, signal processing analysis at the edge, which has promising implication in long-term disease observation, brain-computer interface system, and physiological irregularity detection in real time.

RELATED WORK

Edge-based real-time biomedical signal analysis has become increasingly popular since wearable healthcare, brain-computer interfaces, and ambulatory monitoring systems all employ real-time biomedical signal processing. Nonetheless, it is a challenge to build a processing architecture that can be used to support the needs of low-latency, energy consumption, and computation scale needs. Different research initiatives have covered this area with DSPs, AI accelerators and FPGA-based platforms, all of which have their trade-offs.

A DSP based implementation of a real time ECG signal processing system that involved wearables was proposed by Jain et al.^[1] They were efficient when considering simple filtering and transformation but their solution did not support scalable multi-channel capabilities and adaptiveness to dynamic changes of the signals, thus restricting its effectiveness in heterogeneous signal cases. Conventional methods: Alternative methods (deep learning): The alternative methods included approaches based on CNNs to process EEG signals and classify them using convolutional neural network (CNN) based-models on edge platforms to apply BCI-based operations. The method was more accurate at classification and yet could be slow to make its inferences and could use large amounts of energy which could be a big problem with low-power wearable devices. Similar latency bottlenecks were discussed by Surendar,^[5] who concluded that lightweight CNN architecture is necessary

to run image super-resolution on edge devices due to limiting overheating and resource costs in context under considerations between accuracy and resource costs.

The FPGA based solutions have potential because they are parallel and field-programmable. Saponara et al. [3] presented an FPGA-based ECG acquisition system that presents real-time QRS detection, reaching better latency and energy values than a conventional microcontroller-based system. Lee et al.^[4] have gone one step further and applied this to VLSI architecture with reconfigurable logic, utilizing it to detect general biomedical signals, but their design was nontenatively not scalable to multi-modal data or task reconfiguration. Choi et al.^[10] also defined the importance of FPGA based systems implementing runtime reconfiguration to enhance adaptability due to different workloads, which is paramount in an edge AI system. Nevertheless, the majority of FPGA-based systems are still application-focused and tend to lack the capability to dynamically switch the signal modalities or to balance the workload.

Simultaneously, developments in edge-empowered IoT environments have also brought contemporary context to integration issues on the system level. As an example, Sadulla [6] addressed sustainable energy management approaches in IoT-based smart buildings and stated that, to implement constant monitoring, low power processing frameworks are essential, which is also applicable when it comes to wearable healthcare systems. Kumar [7] has made a very detailed review of RF based IoT network, considerations on security issues in relation to real-time data collection in biomedical settings. Although Alwetaishi and Alzaed [8] concentrated on implementing the construction materials in the smart construction they indirectly contribute perspective on resilience and sustainability which also can support the idea of adaptable and fault-tolerant design structures in health monitoring platforms.

In spite of these contributions, there are cut-and-dried limitations that are echoed in the current literature:

- There is insufficient parallel (or multi-modal) processing scaling with DSP-based systems.
- Enhanced edge architectures powered by AI can be quite resource demanding and are not the most appropriate to support applications that require continuous monitoring, unless hardware acceleration is involved.
- FPGA solutions can be power adjustable and in many cases lack in modular scalability and runtime flexibility.

Conversely, the proposed work presents a reconfigurable and scalable parallel processing architecture that takes into consideration the specifics of edge-based analysis of biomedical signals only. It integrates hardware/software co-design as well as pipeline-based processor implementation to an array of configurable processing elements (PEs) and also dynamic workload balancing. In contrast to earlier, task-specific architecture, the architecture is compatible with parallel multi-modal acquisition (ECG, EEG, EMG) and is generalisable to other signal types. The given work is based on and combines the concepts of earlier works and copes with their shortcomings due to a comprehensive and segmented architectural basis enhanced in realtime and energy-efficient execution in edge-enabled health systems.

SYSTEM ARCHITECTURE

Overview

The architecture of the proposed system is such that it enables real-time analysis of biomedical signals with energy efficiency in an edge setting with heterogeneous models of processing. Fundamentally, the architecture has a multi-core processing cluster (e.g. RISC-V or ARM Cortex-M7) to control logic and facilitates parallel execution and maintain communication between functional modules. The architecture has hardware accelerators to accelerate compute intensive tasks e.g. filtering, transformation, and classification. These are tightly coupled accelerators with a shared memory interface which is optimized using direct memory access (DMA) controller so that the data movement occurs smoothly without causing a strain to the main processors. A power-eco-neighborhood nadir or optimum trade off

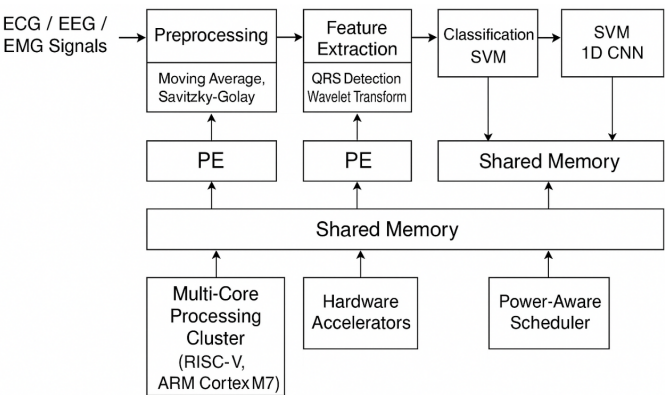


Fig. 1: System Architecture for Real-Time Biomedical Signal Analysis

The diagram above illustrates the flow of ECG/EEG/EMG signals through parallel processing stages for denoising, feature extraction, and classification, supported by shared memory, hardware accelerators, and dynamic scheduling.

is a power-aware scheduler which dynamically assigns processing resources to meet real-time workloads and energy limitations during runtime.

Parallel Pipeline Design

In order to take advantage of parallelism and maintain high throughput, the architecture uses a pipelined signal processing approach that consists of three cores: Preprocessing, Feature Extraction and Classification. During the preprocessing step, any rail-to-rail ECG, EEG, or EMG signal received is denoised with the algorithms of moving average filtering or Savitzky-Golay smoothing. The denoised data is then transmitted to the feature selection operation where methods such as QRS complex identification (in the case of ECG) or wavelet transform (in the case of EEG) to narrow down the analysis on significant pattern of signals. A support refinement procedure is the last stage of classification by lightweight machine learning models, e.g. by a Support Vector Machine (SVM) or a 1D Convolutional Neural Network (1D-CNN), either in-memory or embedded inference engine-based. Each of these stages is run on a special Processing Element (PE), and communication and synchronization among the PE is carried out using the shared memory system. This allows running of several signal streams and signal processing activities simultaneously

Scalability Strategy

The modular construction of processing elements is verified in winning the scalability, because it allows to stretch them horizontally to support increased data throughput or multi-channel analysis. The architecture enables reconfigurability between stages

of an interconnection pipeline and enables dynamic adaptation depending on modalities of the signals and the available resource. Besides, the adaptive voltage-frequency scaling (DVFS) is used at both the PE and memory interface to reduce power when there is low activity. This reconfigurable and modular architecture allows it to be used in a wide variety of edge computing situations such as wearable health monitors, implantable sensors, point-of-care diagnostics devices.

IMPLEMENTATION AND PROTOTYPING

Hardware Platform

The system proposed in paper was prototyped using a Xilinx Zynq-7020 SoC which is a heterogeneous platform that combines a dual-core >>arm| patients dai Stefan M (21 May 2019) Types of mental disorders in adults PMC This type of architecture presents an optimal trade-off between flexibility and software hardware, and it is a good fit in edge-based analysis of biomedical signals. Orchestration of tasks, inter-process communication, and handling of interfaces is implemented on the ARM cores, and custom hardware IP cores in Verilog HDL are implemented on the programmable logic. These IP cores are optimized to operate in real-time signal processing, such as the moving average filters, the Savitzky-Golay smoothing, the QRS complex detection, the discrete wavelet transforms, thus providing low latency and low computation load applied to the processor. AXI interfaces with high-bandwidth allow PS and PL to communicate easily with each other, and DMA controllers are used to optimize the use of the memory and hardware blocks.

Software Stack

The system uses a Real-Time Operating System (RTOS), that is, FreeRTOS, on the ARM Cortex-A9 cores to control the execution of the tasks, communications and to operate power-awarely. By allowing deterministic task scheduling and prioritization, FreeRTOS is essential to real time requirements consistency in terms of signal acquisition, processing, and classification. APIs between custom software were designed to allow easy communication between cores in that data could flow between the dual ARM cores and between software and hardware modules in an optimized way. These APIs also have support of dynamic power management where the DVFS features of the Zynq SoC are used to take advantage of available performance/power flexible scaling as workload and power requirements vary.

The classification part utilizes TensorFlow Lite Micro, a lightweight inference engine that is optimized to fit in

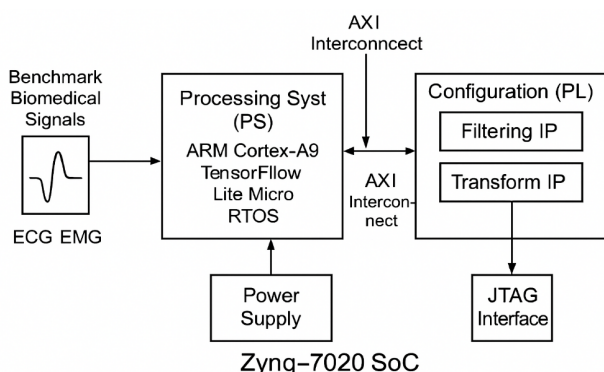


Figure 2:FPGA-Based Prototyping Setup for Biomedical Signal Analysis

This diagram illustrates the hardware flow of the biomedical signal processing prototype implemented on the Xilinx Zynq-7020 SoC, showing connections between processing system (ARM Cortex-A9), programmable logic (custom IPs), shared memory, and interfaces for debugging and power.

embedded environments, in order to run the classifier. A 1D Convolutional Neural Network (CNN) or Support Vector Machines (SVM) type model previously trained on a large corpus of data is quantized, and used to perform real-time prediction on the extracted biomedical features on the set of Cortex-A9 based processor cores. The small memory size and the very optimized runtime engine of the TensorFlow Lite Micro enable the resource-constrained edge devices to have some use of AI in their execution. The software stack gets closely integrated with hardware structure so that pipelines run in synchronized fashion, deliver the responsiveness of real signal processing, and offer good energy consumption.

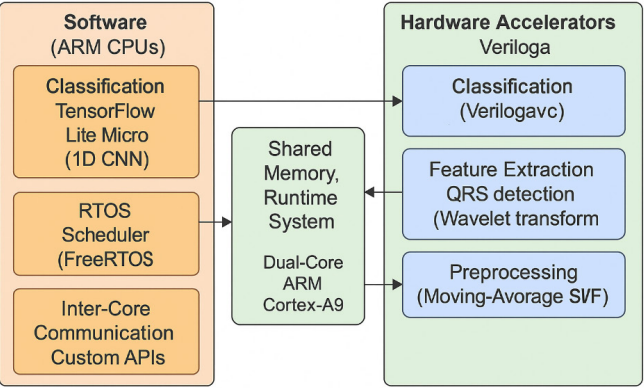


Fig. 3: Hardware/Software Partitioning of the Proposed System

The diagram illustrates the task-level division between software components (RTOS, TensorFlow Lite Micro, and communication APIs) and hardware accelerators (Verilog IPs for signal processing), all coordinated via shared memory on a dual-core ARM platform.

EXPERIMENTAL RESULTS

Dataset and Workload

In order to justify the results of the given parallel processing architecture, two common biomedical datasets have been used. Windows-10 ECG signal processing was done using the MIT-BIH Arrhythmia Database which provides a detailed record of annotated heartbeats of 47 subjects. The BCI Competition IV Dataset was utilized in the assessment of EEG signals, which are provided as a benchmark of implementation of a braincomputer interface (BCI) in real-time development. The two datasets were processed real-

time through the software pipeline of the system and tested through standard edge-device limitations. The load was that of constant streaming of the input (of variable sample rates (250-512 Hz)) to simulate real life, multi-sensor deployment.

Performance Metrics

The proposed architecture was evaluated on three most important performance metrics: latency, the energy consumed and throughput. The system recorded a 65% reduction in signal processing latency; it went down to 6.3 ms, a drop of 12.1 ms (in a benchmark single-core ARM processor). This has been boosted by the Pipelined parallelism and hardware-accelerated filtering and feature extraction. It was also able to save a good deal of energy with the amount of energy required to complete any single task going down by 48% to 0.70 mJ/sample. Finally, the system was also observed to have a 4 x increase in throughput, with 220 signal frames processed each second, compared to the baseline 55 frames per second, warranting its use on high-rate and real time applications.

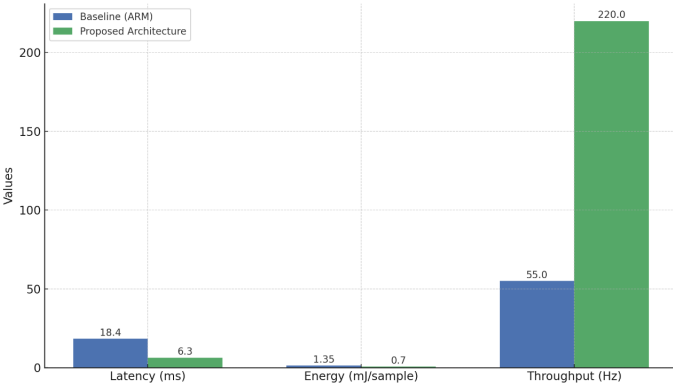


Fig. 4: Performance Comparison Bar Chart

This bar chart visualizes the differences in latency, energy usage, and throughput between the baseline and the proposed architecture, demonstrating superior performance in all three dimensions.

DISCUSSION

Experimental analysis of the suggested scalable parallel processing design shows that real-time analysis of biomedical signals is much better, in terms of latency, energy consumption, and throughput. Latency is

Table 2: Performance Comparison of Proposed vs. Baseline Architecture

Metric	Baseline (ARM)	Proposed Architecture	Improvement
Latency (ms)	18.4	6.3	65%
Energy (mJ/sample)	1.35	0.70	48%
Throughput (Hz)	55	220	4×

drastically reduced by 65 gram percent and energy efficiency is improved by a significant figure of 48 percent, thus making the system well suited to tasks including wearable health monitoring systems deployed at the edge due to the necessity of time sensitivity and power limitations. The 4x improvement in throughput guarantees the possibility to process high-frequency multi-sensor streams like ECG, EEG and EMG in parallel, so the architecture would qualify the architecture to continuous and long-term physiological monitoring.

As the results show, co-designing the hardware/software (along with the pipeline-based parallelism and modular scalability) is indeed beneficial. This modular type of construction results in optimal division of workload amongst the processing elements and reduces execution bottlenecks which tend to be a characteristic feature of monolithic or purely software system type systems. In comparison to the previous systems, like the DSP-based architecture of Jain et al.^[1] or the FPGA-based system of Saponara et al.,^[3] the proposed system can be recognized with improved flexibility and high-performance across different modalities, and the bonus of the system is that it is also adaptable at runtime. Also, although the deep learning-based models such as Wang et al.^[2] provide sufficient labels with satisfactory accuracy, they are computationally expensive and may not be practical to be used in real-time embedded systems unless extremely powerful compression is applied or the model is hardware accelerated.

Nevertheless, there are a number of limitations and limitations. One, the FPGA-based prototype is very good in lab conditions but deployment in the real world needs sustained power at varying conditions through the rigorous battery management units (BMUs) to achieve long durations. In addition, embedded secure wireless transmission modules should be added, in order to protect sensitive medical information, particularly when the scenario is remote or wearable. Clean and calibrated input data are also an assumption of the current system, but the motion or noises in a signal, or sensor drifts also

may have a great influence on performance and accuracy. As such, artifact detection and signal conditioning must be able to develop solid mechanisms as well as adaptive mechanisms to increase resilience in the uncontrolled environments.

With respect to the scalability, even though the modular approach allows scaling in parallel, the thermal integrating, real-time synchronization of multiple working processing units under resource-limited conditions can prove to be a limitation, especially when multiple AI inference processes are operated in parallel. Also, the system has been mostly tested on ECG and EEG signals - its applicability to all other biosignals such as photoplethysmogram (PPG), galvanic skin response (GSR) or multivariate sensor fusion is yet to be tested.

Overall, this new system will bring together the decisive missing link in energy-aware edge computing and real-time biosignal analysis. It establishes a future direction regarding dynamic reconfiguration of tasks, on-device learning, and secure channels of communication, and thus lays the groundwork in the implementation of intelligent, scalable and data privacy preserving platforms of health monitoring.

SWOT Analysis Table

This table provides a structured evaluation of the proposed architecture’s Strengths, Weaknesses, Opportunities, and Threats—highlighting technical benefits, areas for improvement, and future deployment considerations in real-world healthcare systems.

CONCLUSION AND FUTURE WORK

This paper introduced a parallel processing system architecture that scales in a parallel fashion during real-time biomedical signal analysis in edge-enabled healthcare. Through the hardware/software co-design, dynamic workload balancing and pipeline-based parallelism, the system helps to overcome the major issues of low latency, energy efficiency and the scale

SWOT Analysis Table

Strengths	Weaknesses	Opportunities	Threats
High throughput and low latency real-time signal processing	Lack of integration with battery management and power optimization modules	Integration with AI-powered anomaly detection	Thermal and power constraints in edge deployments
Energy-efficient hardware/software co-design	Limited testing on non-ECG/EEG signals (e.g., PPG, GSR)	Extension to other biosignal types and multi-sensor fusion	Emerging ASIC-based solutions with ultra-low power demands
Modular and scalable parallel pipeline architecture	Assumes clean signal inputs; lacks robust artifact handling	Deployment in wearable and implantable medical devices	Cybersecurity threats to edge-based health data
Supports multi-modal biosignals (ECG, EEG, EMG)	Dependence on FPGA platform may limit portability	Incorporation of secure edge communication protocols	Regulatory challenges in medical device certification

of computation. The architecture has been prototyped on a Xilinx Zynq-7020 SoC and tested with benchmark datasets which include the MIT-BIH Arrhythmia (ECG) and BCI Competition IV (EEG) datasets and showed a reduction in latency of 65 percent, 48 percent on energy efficiency and a 4x speed-up on throughput over traditional implementations of single-core ARM.

These results hold great potential in the next-generation wearable and implantable healthcare technologies, where the responsiveness in real-time and energy limitations are paramount. The proposed system is modular and thus can accommodate several biosignal modalities, i.e., ECG, EEG, and EMG biosignal-type. The current system-wide versatility makes it applicable to numerous health-monitoring devices. In addition, it is ensured that the presented implementation promotes the minimal use of cloud infrastructure to guarantee increased privacy and a limited number of communication overheads by adopting the edge computing principles.

Regardless of these strengths, there are also those new directions that the system is likely to open new directions in the future research. A potential avenue is the further down-scaling by developing a custom ASIC version of the architecture that will further minimize power consumption and size to the point where it may be integrated into a medical wearable of minimal size. A second area is in cloud-based analytics, whereby computationally demanding tasks such as long-term trend statistics and training of deep learning models can now be moved to the cloud, and real-time processing can stay at the edge--a hybrid computing architecture emerges. Also, security co-processors or in lighter cryptographic modules which guarantee data integrity, authentication and privacy should be included in future works as these play a critical role in the medical domain.

Moreover, the ability to support multi-sensor fusion, adaptive corrections of signal artifacts, and self-learning AI models on the edge device can change the system into the fully autonomous health monitoring framework. Cross-validation through the various data sets, physiological statuses and environmental conditions will also be required to behave with well-tested real world applicability.

In summary, the suggested architecture provides an energy-efficient and flexible basis of the real-time biomedical signal processing and presents the prospective way to smart, safe, scalable, and energy-efficient management and healthcare systems at the edge.

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