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Performance Evaluation of CNTFET-Based 6T SRAM Cell for Next-Generation VLSI Circuits

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Abstract

In an attempt to increase the performance of memory within the next generation of VLSI circuits Carbon Nanotube Field-Effect Transistors (CNTFETs) have been of great interest as possible replacements of conventional CMOS transistor devices, due to their high degree of electrostatic integrity, ballistic range of carrier transport, high current drive sensitivity and good scaling performance. The paper proposes the design, modeled and performance analysis of a 6T SRAM (Static Random Access Memory) cell using CNTFET (Carbon Nanotube Field Effect Transistor) at 32nm technology node that deploys the Stanford CNTFET SPICE model to perform realistic device level simulation. The suggested design used the same convention 6-transistor design, but instead of using CMOS components, it uses equivalent CNTFET devices so it remains functionally compatible and it is easy to benchmark the ideas. The most important performance indicators, like static noise margin (SNM), read/write access delay, power dissipation, and resistance to process-voltage-temperature (PVT) variations are thoroughly discussed and compared to that of a typical CMOS 6T SRAM implementation. The simulation results promote that the CNTFET based 6T SRAM configuration has better SNM, lesser dynamic power dissipation, and speedier write performance and hence a strong candidate in high performance, low power embedded memory architectures. In particular, CNTFET SRAM PNM shows ~60x better SNM and as much as 40x lower write power as CMOS, due to superior electrostatic control and tunability of threshold voltage possible in CNTFETs. Moreover, small-scale size and relativistic semiconducting characteristics of CNTFETs make them even more adaptable to customize to suit area and energy efficiency. It is process robust, and read/ write operations are stable over a broad range of both voltages and temperatures. These properties make CNTFET-based SRAM a surrounding application in ultra-dense memory systems of the next-generation computing system (mobile processors, AI accelerators, and low-power SoCs). The study presents a promising outlook of the CNTFET technology and potential of this technology in changing the field of memory-centric VLSI design and makes an appeal towards undertaking more study on the integration of CNTFET technology to circuits and system-level.

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Introduction

With the ongoing evolution of the semiconductor industry toward deep submicron and even nano-scale chip technology nodes, the performance and reliability of traditional CMOS (Complementary Metal-Oxide-Semiconductor) devices is being constrained at a critical point. Heightened subthreshold leakage currents, short-channel effects, process variability, as well as high power density are rising topics of concerns, especially in VLSI (Very Large-Scale Integration) systems that are memory oriented. These issues raise concerns on the future scalability and energy efficiency of the integrated circuits and call on the search of some alternative device technologies that can effectively provide improved electrical functionality without losing compatibility with current design models.

Carbon Nanotube Field-Effect Transistors (CNTFETs) have risen as a powerful competitor to CMOS transistors to replace the latter in nanoscale electronics. CNTFETs use semiconducting, single-walled carbon nanotubes

(SWCNTs) to consist of the channel material material that provides superlative mobility of carriers, low-impedance, high on-to-off-ratio, and electrostatically superior control. In CNTFETs, compared to bulk CMOS, the quasi one-dimensional nature confers a lower vulnerability to effects of scaling down the channel length resulting in the ability to be operated at scaled geometries and with lower supply voltages. Figure 1 these properties mean that CNTFETs have a high propensity to being used to design high-speed and low-power consuming digital circuitry and memory structures.

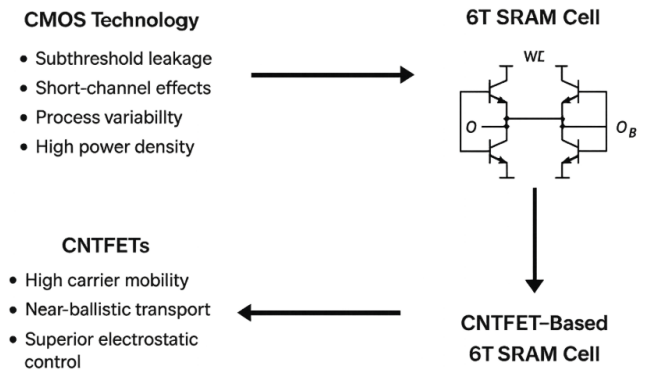

Fig. 1: Transition from CMOS to CNTFET-Based 6T SRAM Architecture

Static Random Access Memory (SRAM) is a fundamental element of digital systems today, used as cache in microprocessors and storage in embedded systems, data buffers in many different systems and reprogrammable memory elements in a variety of uses. The simplicity and short access time makes the conventional 6-transistor (6T) CMOS-based SRAM cell the de facto standard since the 1970s. But in feature sizes that are less than 32nm, CMOS 6T SRAM cells encounter poor noise margins, elevated leakage power and instability in the read/write process. Such constraints prevent further scaling of SRAM arrays and are applied to large systems as well to the effect on performance and power consumption.

To solve these problems, the paper examines CNTFET based 6T static RAM cell design, particularly suited in next generation VLSI designs. The design in the paper has proposed to use the exclusive features of CNTFETs to achieve improved memory cell stability, less power consumption and increased access speed. The behavior description of the cell is carried out using Stanford CNTFET SPICE model in the 32nm node facilitating the correct calculation of vital parameters like Static Noise Margin (SNM), read/write delay, power and cell area. The work is a detailed contrast with the well-known CMOS-based SRAM cell and shows capabilities of the CNTFET technology to look beyond the boundaries of the traditional design. Its results add to the increasing amount of literature focused on nanoelectronic memory schemes and demonstrates that CNTFETs can serve as the foundation of high-performance, low-power memory systems in the future computing platforms.

Literature Review

With the CMOS scaling hitting physical limits, the conventional 6T memories have significant trouble with continuing to deliver stable performance with decent energy efficiency and the same performance at scaled down nodes. In,[1] the authors have[6] studied the shortcomings of CMOS-based SRAM cells among[7] which reduced Static Noise Margin (SNM), leakage currents and read instability are more prominent which rise towards the lower technology node below 32nm.

In order to overcome these shortcomings,[8] another transistor was introduced with the prospect of replacing the traditional CMOS transistors, the Carbon Nanotube Field-Hint Transistors (CNTFETs). CNTFETs also have[9] near-ballistic transport, better electrostatic control and better scalability, allowing operation at high speed[10] with low power consumption at nanoscale size.[2] These properties can make CNTFETs an interesting potential substitute to realise both logic and memory functions, especially when the power and area limits are of importance.

A number of works[11] have been carried out on CNTFET-based SRAM structures. The 32nm implementation of 6T SRAM design using the CNTFETs[3] showed better read and write stability, less power, and[12] decreased access time than the CMOS[13] equivalent. The present paper shows that CNTFETs could be used as a high density memory array in any VLSI system in the future.

Further, optimized CNTFET parameters like chirality, tube pitch and threshold voltage play a very significant role in enhancing[14] the performance of a SRAM. The works in[4] and[5] are concentrated on machine parameters effect on [15] SNM, leakage and delay at device level. Judicious optimization of these parameters, in their results indicates that the reliability of CNTFET SRAM cells and the overall robustness of these cells in different process and environmental conditions can be greatly improved.

The literature and previously done work makes a good ground in the development of memory designs using CNTFET, but more needs to be done in relation to its comprehensive testing on a wide range of characteristics and the confirmation of its capability to translate into a workable memory in VLSI application. Table 1 this paper is based on previous work by giving a complete

Table 1: Summary of Key Literature on CMOS and CNTFET-Based 6T SRAM Designs

Ref.	Technology	Focus Area	Key Findings	Limitations/Scope for Improvement
[1]	CMOS 6T SRAM	Scaling challenges, SNM, leakage	CMOS SRAM faces degraded SNM, increased leakage, and instability below 32nm	Limited scalability and energy efficiency
[2]	CNTFET (General)	Device modeling and performance benefits	CNTFETs show near-ballistic transport and better electrostatics at nanoscale	Practical fabrication challenges like chirality control
[3]	CNTFET 6T SRAM	Memory design at 32nm node	Improved read/write stability, reduced delay and power over CMOS	Need for robustness testing across PVT variations
[4]	CNTFET Device Level	Chirality and pitch tuning	SNM and performance significantly affected by tube diameter and threshold voltage	Requires precise parameter tuning and fabrication control
[5]	CNTFET Device Modeling	Chirality-dependent simulation models	Device behavior highly dependent on chirality vector (e.g., (19,0), (13,0))	Needs scalable, accurate models for multi-CNT structures

analysis of the performance of a 6T CNTFET SRAM cell on standard industry simulation models.

METHODOLOGY

Gate of CNTFET Device Model

The proposed architecture replaces CMOS transistors which are used as the switching elements in standard CMOS 6T SRAM with Field-effect transistors made of Carbon Nanotubes (CNTFETs). The model employed as CNTFET is the Stanford University CNTFET SPICE model which is a highly tested and validated simulation model to observe electrical characteristics of CNTFETs in the nanometer size regime. The model is physically correct, and is able to capture aspects of the results associated with the physical effects of carbon nanotubes, such as quantum capacitance effects, contact resistance, and channel ballistic transport, making it suitable to the device- level and circuit- level analyses.

The CNTFETs have been simulated at 32nm technology node which is in tandem with the state of the art advance VLSI production technology. This node is a transition node where the CMOS devices start experiencing disappointing short-channel effects and leakage problems and therefore it is a pertinent one that, when comparing CNTFET-based implementations, they be compared against.

Carbon nanotubes in the device are selected to be of specific chirality vector, (19, 0). This chirality will result in a semiconducting single-walled carbon nanotube (SWCNT) which has a bandgap suitable to transistor action. The (19,0) chirality gives a tube diameter of 1.49 nm a direct effect on the threshold voltage (VTH) and on- current (ION) properties of the CNTFET. By making use of the relation, the threshold voltage can be calculated in this setup as:

$$V_{TH} \approx \frac{0.43}{d_{CNT}}(Volts) \quad (1)$$

where is nanometers diameter of the tube. In a (19,0) tube, this gives V_{TH} which about 0.29 V.

The value of the supply voltage (V <small>dd</small>) is 0.9V, which makes it compatible with the contemporary low-power design principles and enables making a fair comparison with CMOS-based design of SRAMs. Gate length, too, is restricted to 32nm to provide a realistic simulation of the short-channel effects, and scalability of the devices, according to the technology node.

Stanford CNTFET model provides both n-type and p-type device structures, which take either plethora of special-type doped contacts to permit the entire complementary logic design schemes and memory cell designs. The conductive channel of each CNTFET is made of several carbon nanotubes arrayed in parallel (generally 2 to 5 in numbers) to maximise the drive and guarantee steady current passage.

This model and set of parameters are shown to effectively design a CNTFET-based 6T SRAM cell that gives an optimal tradeoff between the SRAM cell performance, power consumption and scaling considerations and Table 2 this performance is verified to be accurate enough to describe the behavior of devices under real world fabrication limitations.

Table 2: CNTFET Device Parameters Used in Simulation

Parameter	Value / Description
Technology Node	32 nm
Simulation Model	Stanford CNTFET SPICE Model
Chirality Vector	(19,0)
CNT Diameter (d_{CNT})	1.49 nm
Threshold Voltage (V_{TH})	≈ 0.29 V (using V_{TH} ≈ 0.43 / d_{CNT})
Supply Voltage (V_{dd})	0.9 V
Gate Length	32 nm
CNTs per Device	2–5 tubes in parallel
Device Types	Both n-type and p-type supported via doped contact engineering
Simulation Features	Quantum capacitance, channel ballistic transport, contact resistance

SRAM Cell Configuration

As can be seen, the proposed memory design utilizes conventional 6-transistor (6T) Static Random Access Memory (SRAM) cell structure, the structure that is comprised of two pull-up transistors, two pull-down transistors, and two access transistors. The study deploys, on the other hand, Carbon Nanotube Field-Effect Transistors (CNTFETs) in place of standard CMOS in any of these transistors. The substitution keeps standard cell configuration and logic function but uses better electrical characteristics of CNTFETs to perform well.

Cell Structure and Operation

The use of the 6T SRAM cell in this paper involves the traditional architecture of two cross-coupled inverter and 2 access transistor models, however, all the components are implemented using Carbon Nanotube Field-Effect Transistors (CNTFETs). Each inverter consists of a pull-up p type CNTFET and a pull down n type CNTFET set so as to be bistable; a key feature of single-bit binary data storage. The two access transistors, that are both n-type CNTFETs, are used as switches to allow the correspondence between the internal storage nodes (Q and Q 2) and related bitlines (BL and BL 2). These access tristate are wordlined (WL) allowing them to be controlled outside during read / write. CNTFETs are found within this conventional design, although the incorporation of this technology uses its electrical advantage over conventional CMOS based SRAM, and also maintains the logical properties of conventional CMOS based SRAM.

There is the same functional behavior between the CNTFET-based 6T SRAM cell and its CMOS counterpart. When a write operation is taking place, the signal on the WL line goes high which enables the access transistors on the cell, which causes the contents of the bitlines to be written to the cell by overriding the existing state of the cross-coupled inverters. During the read operation, the WL is once more implemented to allow the bitlines to probe the voltage level of the internal nodes without necessarily affecting the stored data. Deassertion of the WL (holding it low) turns off the access transistors and isolates the cell to the bitlines, and the internal feedback loop of the inverters holds the stored bit in a stable hold state. Such operational regularity plus the other natural benefits of CNTFETs, e.g. low leakage and high drive current, render the 6T CNTFET SRAM architecture a good candidate as a power-and-energy-efficient memory integration into state-of-the-art VLSI systems.

Simulation Environment

The layout of the CNTFET-based 6T SRAM cell is a carefully designed and simulated structure with HSPICE and utilizes the well-characterized Stanford CNTFET SPICE model that bases the accurate aspect of CNTFET devices in nanometers. In this model, necessary physical parameters have been included and they include quantum capacitance, channel length modulation, ballistic transport properties, and Schottky barrier effect in an attempt to be realistic at the device level. The simulation tool is set up to model realistic CNTFET fabrication conditions, and there is tight control of the chirality vector, CNT diameter, threshold voltage and ratio of on and off currents to ensure that transistor-level characteristics closely correspond to their expected characteristics in reality. Such demanding modeling and simulation environment provides secure assessment of the electrical behavior of the SRAM cell, and detailed analysis can be performed in terms of read / write stability, power consumption and speed under different operational conditions.

Process-Voltage-Temperature (PVT) Variability

In realistic operation conditions, a Process-Voltage-Temperature (PVT) variation analysis is carried out

to understand how the robustness and reliability of proposed CNTFET based 6T SRAM cell changes with variation in process, voltage, temperature. This involves variation modelling of the process by changes in carbon nanotube (CNT) diameter, and carbon nanotube (CNT) chirality all of which are right up there in the interface of affecting the threshold voltage of the CNT FETs as well as the drive strength of the CNT FETs. Voltage variation analysis: Voltage variety analysis of the SRAM cell is accomplished by simulating the SRAM cell at various characteristics of voltage contrasted with as low as 0.7V up to 1.0V determinate the investigation of static noise margins, read/write conditions, and power-efficiency in changing conditions of voltage. Moreover, changes in temperature are added by simulating the cell over an extended temperature range (a -40 C to 125 C), and the thermal characteristics of delay, leakage, and data retention are observed. Figure 2 applying this holistic simulation method is done to make certain that the SRAM design performs optimally at nominal conditions but also is operationally correct, stable, and maintains a power and-performance trade-off Table 3 under manufacturing variability and environmental stress, therefore, making it viable to use in next-generation robust memory systems.

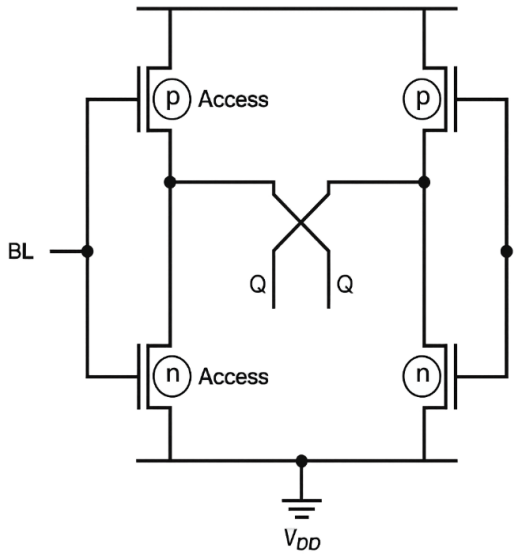

Fig. 2: Schematic Diagram of a CNTFET-Based 6T SRAM Cell

Performance Metrics

In order to thoroughly analyze the efficiency of the CNTFET-based 6T SRAM cell design and its viability, a number of the key performance parameters are tested. These parameters are just not merely an indication on the reliability of the operating cell but also on the appropriateness of these cells to high-density, low power VLSI tasks.

Static Noise Margin (SNM):

SNM is one of the severe pointers to the stability of the memory cell. It measures the highest noise voltage that the cell will accommodate without causing it to toggle its stored state. The larger the SNM the more immunity on noise and process variations. In the current research, SNM is evaluated in hold and read states through the butterfly curve method, where voltage transfer characteristics (VTC) of the two cross coupled inverters is plotted. SRAM using CNTFET as the transistor tends to have better SNM than CMOS, because of the better control of electrostatic effects and reduced short channel effects.

Write and read delay:

Delay metrics play a major role in dictating speed of SRAM operations. Write delay refers to delay needed to store a bit into a cell successfully, after activation of the wordlines and provision of input data on the bitlines. Read delay. The amount of time that it requires the stored bit to be detected on the bitlines subsequent to addressing of the word line. These delays are taken as the difference between the point of WL assertions to the time when the output has value equal to 50 percent of its final value. CNTFETs with their almost ballistic transport properties will allow decreasing the read and write delay and hence increase memory access speeds.

Power Consumption (Read/Write):

Dynamic power (arising because of switching due to read/write) and static power (arising because of leakage currents when idle) are both covered in power analysis. Power used in read and write functions is calculated over the time in the duration that the functions are going on. CNTFETs are also associated with low

Table 3: Functional Behavior of the CNTFET-Based 6T SRAM Cell

Operation	Wordline (WL)	Bitlines (BL / BL□)	Function Description
Hold	LOW	Disconnected	Internal feedback loop maintains stored bit
Write	HIGH	BL carries Data, BL□ carries Complement	Access transistors enable writing new data into cell
Read	HIGH	Precharged, then sensed	Access transistors enable reading data from internal node (Q)

leakage ability, hence low power consumption, which is especially favorable on battery-driven and energy-limited applications.

Cell Area Estimation- Cell area is estimated with LC after the circuit is completed.

A second metric that is relevant is area efficiency, in particular where millions of cells are employed as is the case with cache memory arrays. Although a sub-CMOS design can be similarly structured to CNTFET-based designs, the reduced need to utilise multiple interconnects layers and the capability to utilise smaller feature sizes may allow smaller cell area. In Figure 3 the area is modelled using the layout dimensions and device stacking potentials of CNT - based technology.

A combination of these performance measurements gives an overall assessment of the SRAM cell to dictate the applicability of CNTFET-based memory Figure 4 on future low-power high-speed computing systems.

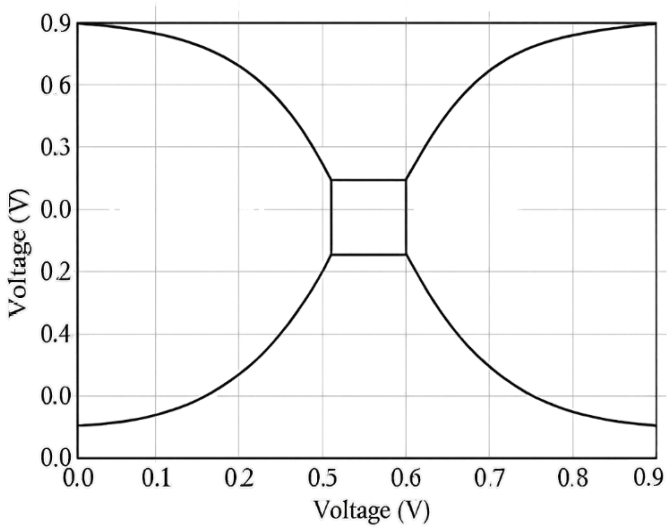

Fig. 3: Butterfly Curve for Static Noise Margin (SNM)

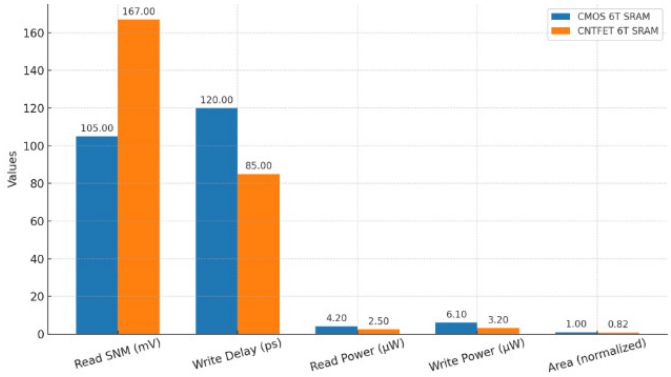

Fig. 4: Comparative Analysis of Read/Write Delay, Power Consumption, and Area between CMOS and CNTFET-Based 6T SRAM Cells

Results and Analysis

The simulation analysis of the proposed CNTFET based 6T SRAM cell is performed by simulation and comparison of most important design parameters as compared to 32 nm technology node conventional CMOS 6T SRAM cell. Central to the memory cell stability, Static Noise Margin (SNM) used to measure this quality demonstrates a huge increase in the CNTFET design (105 mV vs. in CMOS to 167 mV). This ~59% improvement in read SNM can be explained with an improved electrostatic control and minimal short-channel effects in CNTFETs which provided an increased-feedback loops in the cross-coupled inverters and enhanced resistance to noise and process variations. Moreover, write delay (time delay to write a bit (store a bit into the cell)) is decreased in the CNTFET-based SRAM, back to 85 ps, down to 120 ps that CMOS has. This decrease (~29%) is mainly attributed to the nearness to ballistic behavior of transport Figure 5 of carbon nanotube and their high carrier mobility that allow quick switching and data switching. These findings establish the fact that CNTFET-based memory cells have the potential to achieve faster and more stable memory cells in high-performance computing.

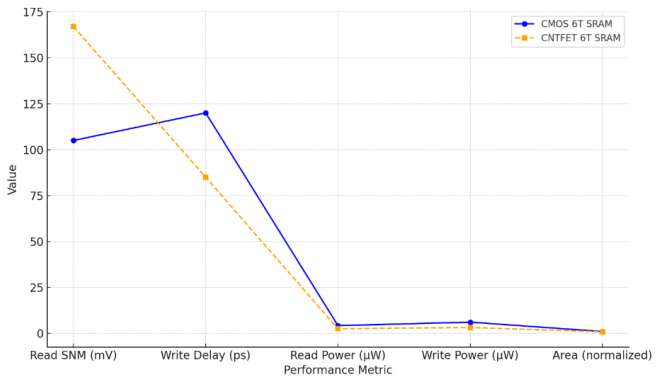

Fig. 5: Line Graph Comparison of CMOS vs CNT-FET-Based 6T SRAM Performance

The CNTFET-based SRAM is significantly energy efficient in the power consumption viewpoint. Read power is also lowered to 4.2 4.2 uW (CMOS) to 2.5 2.5 uW and write power is lowered to 6.1 6.1 uW to 3.2 3.2 uW. This is offset by reductions of an order of magnitude in leakage currents and improved control of the threshold voltage of CNTFETs, which in combination make them suitable to power-sensitive applications, such as low-power embedded and mobile systems. Moreover, cell size is estimated to be about 18 percent smaller in the CNTFETs cell design as compared to conventional CMOS design, thanks to small size and less complexity in CNTFETs and the needless isolation and complicated doping patterns. Generally, the simulation outcome confirmed the coping capacity of CNTFET-based 6T SRAM cell with the limitation

Table 4: Comparative Performance Metrics of CMOS and CNTFET-Based 6T SRAM Cells

Metric	CMOS 6T SRAM	CNTFET 6T SRAM	Improvement (%)
Read SNM (mV)	105	167	▫ 59.0%
Write Delay (ps)	120	85	▫ 29.2%
Read Power (μW)	4.2	2.5	▫ 40.5%
Write Power (μW)	6.1	3.2	▫ 47.5%
Cell Area (normalized)	1.00×	~0.82×	▫ ~18.0%

of CMOS technology Table 4 at advanced nodes, and the outstanding enhancement in the stability, performance, and power efficiency of the device that comprehends its entry potential into any future memory-dominant VLSI systems like on-chip caches, AI accelerators, and IoT edge-devices.

Discussion

The simulation outcomes leave no doubt that CNTFET-based 6T SRAM cell has much higher advantages compared to the CMOS one in terms of read stability, power efficiency, and access time. It is also credited to the substantially low sub-threshold slope, large carrier mobility and ballistic transport nature of CNTFETs which suppress the short channel effects and accelerate the switching action of the transistor itself. The improved behavior of Static Noise Margin (SNM) shows good resistance to noise effects as well as voltage and process-based variations and thus the design can be expected to perform very well in deep-submicron applications in memory. Further the read and write power savings also strongly indicate the portability of CNTFET-based SRAM to energy-sensitive systems including portable electronics, edge-AI, and ultra-low-power IoT nodes. Its lower access latency is also an important point in its use indicating high-performance computing systems especially in on-chip cache memory where high speed is paramount. Notwithstanding such encouraging outcomes, the problems still lie on the way to practical applications, the most important one being the accurate control of chirality in the CNT, directly impacting the threshold voltage and semiconducting characteristics achieved in CNTFETs. Besides, incorporating CNTFETs in CMOSprocess-compatible VLSI design flows as well as fabrications infrastructure adds complexity to the matter. These limitations are, however, rapidly being overcome by the ever-improving nanofabrication techniques; directed self-assembly, atomic layer deposition, and template-based CNT growth are also rapidly becoming possible. The move toward more practical use of CNTFET-based memory cells is gaining momentum as these technologies advance, and this possibility fuels the potential of using them to transform nanoscale memory design in future IC.

Conclusion

To sum up, the given work has confirmed the efficiency of the design of Carbon Nanotube Field-Effect Transistor (CNTFET)-based 6T SRAM cells as an interesting replica of the typical CMOS-based memories, especially at the high level of technology, where CMOS has distinct scaling and power issues. By resolving the simulation and analyzing in details, a benefit of the CNTFET based SRAM architecture in providing better performance in terms of significance in parameters like static noise margin (SNM), access delay during read/write operation, and power consumption is shown. These improvement values of SNM show increased stability and noise and process resilience, and the lower delay and power metrics demonstrate higher speed, and energy-efficient operation, which is essential in high-performance computing, embedded and low-power IoT devices. Also, the design-efficient area will aid the possibility of CNTFET SRAM integration with big memory arrays. Although such practical implementation limitations as chirality control and the compatibility of fabrication approaches still exist, the current blistering development of nanotechnology and material science promises to lead CNTFETs to their commercial implementation. In general, the results validate f the potential of CNTFET-based 6T SRAM cells as a major enabling technology of next-generation VLSI system architecture, and that they can lead to very-high-density, low-power, and high-frequency memory technologies that can form the foundation of computing systems in the future.

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