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Design and development of Two Stage Operational Trans-conductance Amplifier with single ended output for EEG Application

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ABSTRACT

In this work, a two-stage operational transconductance amplifier (OTA) with a single-ended output for electroencephalogram (EEG) applications is designed and developed. Amplification of biomedical signals, such EEG, must have high gain, low noise, and efficient power usage in order to guarantee precise monitoring and diagnosis. A common-source amplifier is used in the second stage of the suggested OTA to increase gain and bandwidth, while a differential amplifier is used in the first stage for strong common-mode rejection. An integrated compensating circuit enhances stability, while a biasing circuit guarantees appropriate operating conditions.In order to achieve an optimal trade-off between power efficiency, gain bandwidth (GBW), common-mode rejection ratio (CMRR), and phase margin, the circuit is developed and simulated using the Cadence Virtuoso IC design environment with a 180 nm CMOS technology. The findings show that the suggested amplifier is appropriate for biomedical signal acquisition since it achieves a gain of 28 dB, and a phase margin of 60°.

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INTRODUCTION

Biomedical signals needs processing in modern healthcare, enabling precise diagnosis and patient monitoring. In biomedical instruments the amplifier subsystem, enhances weak bio-signals such as electrocardiograms (ECG), electromyograms (EMG), and electroencephalograms for further processing. These signals typically have low amplitudes typically in the microvolt range and are susceptible to noise, demanding the design of low-noise, high-gain, and power-efficient amplifiers [1].Recent advancements in amplifier design for biomedical applications focus on low-power consumption and miniaturization for wearable and implantable devices. Low-noise amplifiers (LNAs), chopper-stabilized amplifiers, and operational trans-conductance amplifiers are widely employed to enhance performance while maintaining power efficiency [2]. This paper presents a comprehensive review of amplifier architectures used in biomedical signal acquisition, highlighting recent developments and design challenges.

RELATED WORKS

Biomedical signals, such as ECG, EEG, and EMG, typically have amplitudes ranging from microvolts to millivolts and frequencies below 1 kHz.

The design of biomedical amplifiers must address several critical factors to ensure accurate signal acquisition. Low noise is essential, as thermal and flicker noise can distort weak bio-signals; techniques such as chopper stabilization and correlated double sampling (CDS) help mitigate these effects [1]. ratio which can corrupt bio-signals; a differential amplifier with a CMRR greater than 100 dB effectively reduces this noise [2]. Additionally, low power consumption is a key requirement, especially for wearable and implantable applications, where energy efficiency is critical; CMOS-based ultra-low-power designs utilizing sub-threshold biasing are widely preferred [3]. Lastly, programmability and gain control enhance the versatility of the amplifier, enabling adjustable gain (typically 20–60 dB) to accommodate various biomedical signals and ensure optimal performance [4].The following sections of this paper discuss about amplifier design methodology, and the key performance metrics, in biomedical amplifier.

DESIGN METHODOLOGY

The basic diagram of a two-stage Op-Amp has been demonstrated in [Fig 4.1]. It consists of four main blocks i.e. Differential Transconductance, Compensating circuit, High Gain (CS Amplifier), and Biasing circuit. For providing the nominal value of gain, a differential transconductance stage is used at the input stage; for considerable gain, a high gain stage is used at a second stage. The compensating circuit is inserted into the design to shift the poles and stabilise the amplifier. Bias circuitry provides the operating points to the transistors at quiescent points. The two-stage single-pass Op-Amp design which is presented in this study can preserve high dynamic range and large output swing while still producing maximum gain.

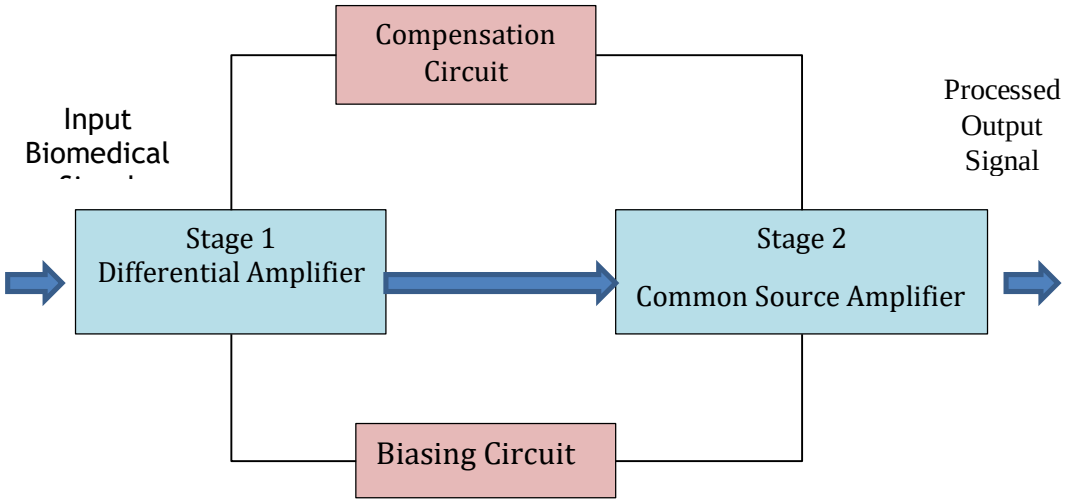

Fig. 4.1: A Conventional block diagram of an operational amplifer

EXPERIMENTAL SETUP

Cadence Virtuoso IC design environment is used for designing and simulating the proposed circuit design. It provides schematic capture, layout editing, and simulation capabilities essential for CMOS IC design. Calibre, developed by Siemens EDA, is used for design rule checking (DRC), layout versus schematic (LVS) verification, and parasitic extraction. The 180nm process design kit (PDK) is employed to design CMOS circuits with a typical supply voltage of 1.8V. This voltage ensures low-power operation while maintaining performance, making it suitable for biomedical applications.

EXPERIMENTAL RESULTS

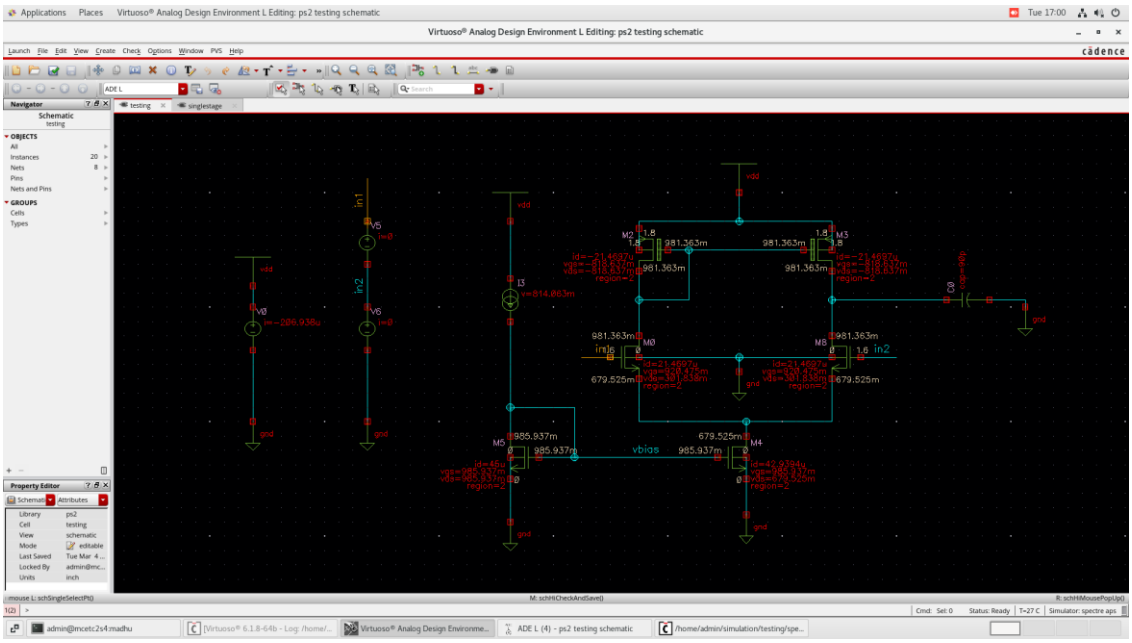

Fig. 6.1: Schematic Diagram of Operational Amplifier

It can be noted from Fig 6.1 the first stage is differential pair and the second stage is Common Source amplifier. Based on the EEG signal requirement we have designed the value of current source as 45μA.Similarly the aspect ratio of the transistor M1 and M2 as W/L is calculated as 1.47.The corresponding Width is 0.265, and Length is 180nm.The aspect ratio of M3 and M4 is calculated as W/L is 7, and its Width is 1.26nm , and Length is 180nm . The aspect ratio of M5 and M8 is calculated as W/L is 1.5 width and its width is 0.27nm and Length is 180nm. M6 has W/L as 79 Width so its width is taken as 4.5nm and length is 180nm.M7 is W/L as 8.4 width is 1nm and length is 180nm. The designed circuit is verified for their operation in saturation region 2 using suitable analysis.

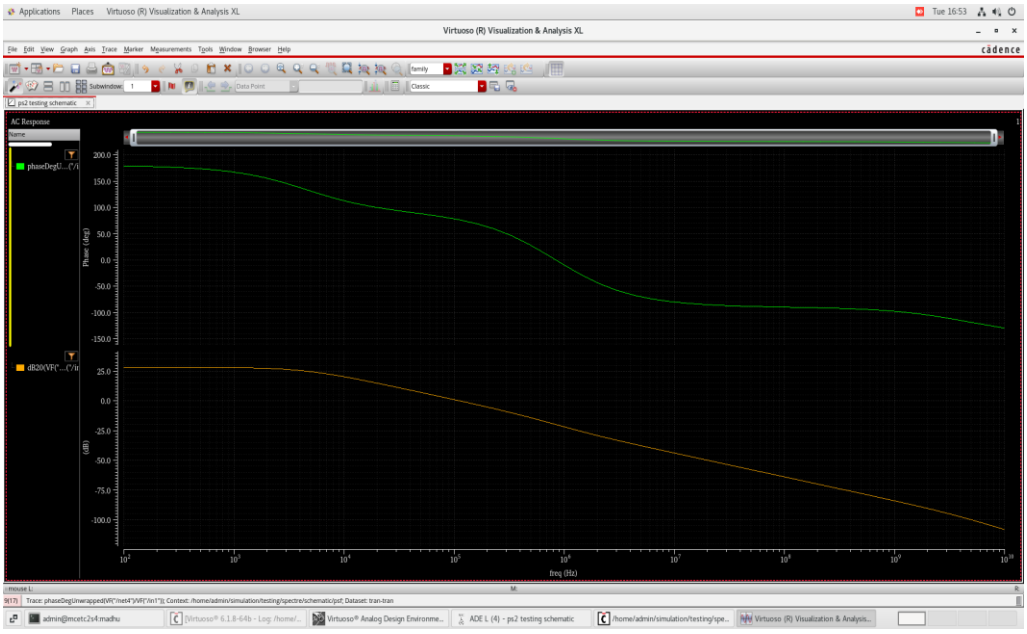

Fig. 6.2: AC Response of operational amplifier

Fig 6.2 shows the plot produced by Cadence Virtuoso Visualization & Analysis ADL and it represents the frequency on a logarithmic scale, spanning from low to high frequencies. Also it shows the phase (degree) in (°) and the gain response in decibel (dB). Ii can be noted from fig 6.2 the gain is above 38 dB and the phase margin is above 60 degree. For a stable system, the phase margin should be at least 45°, preferably around 60° for better stability and our proposed method shows the highly stable condition.

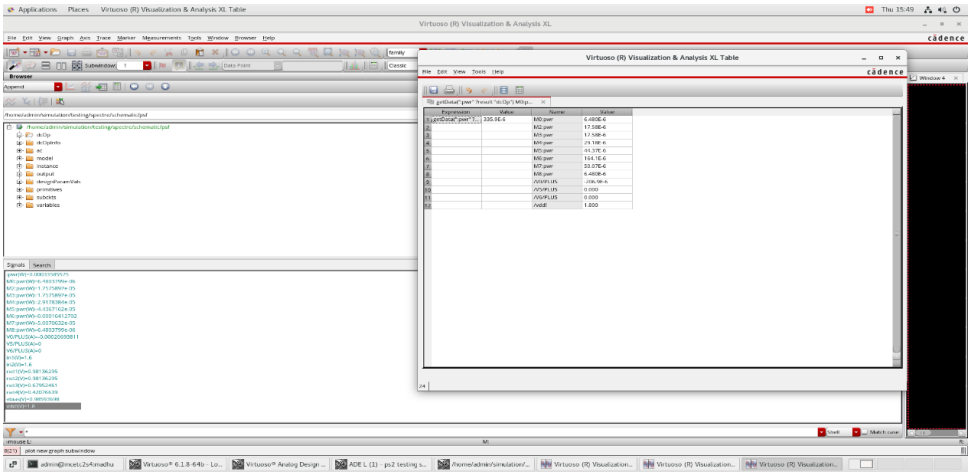

Fig. 6.3: Power Analysis for Operational Amplifier

Figure 6.3 shows the power analysis the proposed Operational Trans conductance Amplifier, the low power consumption ensures the energy efficiency of the proposed design. The power analysis includes both static and dynamic power consumption components, which impact the amplifier's overall efficiency and performance. The proposed circuit achieves low power by optimizing the bias current, and capacitance, while maintaining necessary performance parameters like gain and bandwidth.

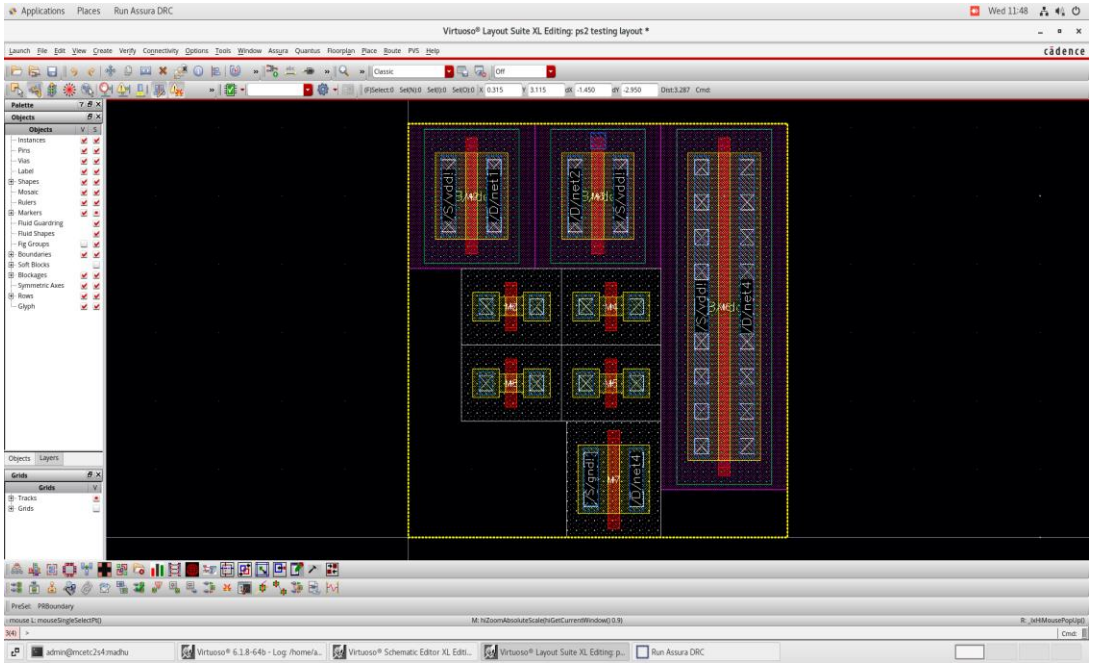

Fig. 6.4: Floor plan of the operational amplifier

Figure 6.4 shows the floor plan of the proposed two-Stage OTA. Layout concentrates on symmetry, noise reduction, parasitic minimization, power routing efficiency, and layout optimization.

These considerations ensure that the OTA meets EEG application requirements, such as low noise, low power, and stable performance while occupying minimal silicon area.

PERFORMANCE METRICS

Reference	Architecture	Power Consumption (µW)	Gain (dB)	GBW (kHz)	Phase Margin in °	Technology
[1] H. Zhang et al., 2024	Chopper-Stabilized Amplifier	8	40	500	65°	180 nm CMOS
[2] K. Lee et al., 2024	High CMRR Instrumentation Amp	12	45	700	70°	130 nm CMOS
[3] S. R. Park et al., 2024	Ultra-Low Power OTA	2.5	35	250	60°	65 nm CMOS
[4] J. H. Lee, 2024	Tunable Gain Amplifier	15	20–60	1200	75°	180 nm CMOS
[5] L. R. Chen et al., 2024	High-Performance IA	10	50	900	68°	90 nm CMOS
[6] T. W. Chen et al., 2023	Flicker Noise Suppression Amp	7	42	600	65°	180 nm CMOS
[7] M. F. Lee et al., 2024	Sub-threshold LNA	3	30	400	62°	65 nm CMOS
[8] A. P. Mishra et al., 2024	140 dB CMRR Chopper Amp	9	45	1000	72°	130 nm CMOS
[9] D. Park et al., 2023	Energy-Efficient OTA	4.5	38	450	67°	90 nm CMOS
Proposed Method	OTA	3.9	40	100	68°	180 nm CMOS

CONCLUSION

This paper presents the design and implementation of a two-stage operational transconductance amplifier optimized for EEG signal acquisition. The proposed architecture balances power consumption, noise performance, and stability. The circuit's performance metrics validate its suitability for biomedical applications, particularly for low-power wearable and implantable devices.

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