Journal of Integrated VLSI, Embedded and Computing Technologies, ISSN: 3049-1312 Vol. 2, No. 1, 2025 (pp. 46-52)
RESEARCH ARTICLE ECEJOURNALS.IN

Energy Efficient VLSI Design for Next Generation IoT Devices

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Keywords:
Energy-Efficient VLSI;
Low-Power Design;
IoT Device Optimization;
VLSI Circuit Design;
Sustainable Electronics

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DOI: 10.31838/JIVCT/02.01.06

Received : 18.11.2024
Revised : 20.12.2024
Accepted : 18.01.2025

Abstract

Mankind has turned into an era where our environment will gradually accept a place to modify how we connect to it, the Internet of Things (IoT). This technological shift is based on the critical requirement of energy efficient Very Large Scale Integration (VLSI) circuits. These are the same circuits as the core of the IoT edge circuits to receive, process, and transmit data in the minimum power consumption. Now that is the demand for low power VLSI solutions in the emerging world of IoT ecosystem. The authors discuss in this article the design intricacies of VLSI circuits intended for the special applications in the IoT. On the way we will discover emerging technologies, new ideas and exciting breakthroughs in the field of energy efficiency. Other strategies to make IoT hardware better: none shall be spared, and we will go from architectural innovations to circuit level optimizations, and beyond. In this comprehensive guide, readers will learn about the challenges in low power VLSI design for IoT, what are these solutions and how IoT future will look like. Now, if you are a engineer, researcher or a tech enthusiast this article presents some very useful tips on how to start designing energy efficient IoT hardware.

How to cite this article: Al-Saud F, Al-Farsi M (2025). Energy Efficient VLSI Design for Next Generation IoT Devices. Journal of Integrated VLSI, Embedded and Computing Technologies, Vol. 2, No. 1, 2025, 46-52

The IoT revolution and the need for low power VSLSI

In the context of the proliferation of IoT devices, industries and daily life have passed through little short of revolution. However, IoT technology is becoming ubiquitous: smart homes, industrial automation and so on. But such rapid expansion comes at a big price: power consumption.[1]

An Analysis of the Power Predicament in IoT Devices

Mostly, the IoT devices work in harsh and diversified ambiances such as where the access of continuous power sources is hindered. The design and functionality of many of these devices rely on batteries or energy harvesting techniques, and hence their power efficiency is the critical factor in the design of the system. In order to enable ultra low power and tight power aware solutions while with very low energy footprint and high battery life of IoT networks, hardware designers have a tremendous pressure.

VLSI Circuits: The Unsung Heroes of IoT

At the heart of every IoT device is, however, VLSI circuits. These integrated circuits handle data processing, communications control, and other various functions of this device. To cater to the increasing need of more sophisticated IoT applications, the circuit with an increasing complexity is required. As the system increases in complexity, power consumption is high, therefore, there is a high design challenge (Figurre 1).

Balancing Power Consummation vs. Performance

The main challenge of designing VLSI circuits for IoT applications has been that such a balance between performance and power consumptions is difficult to achieve. IoT devices have to become more capable of performing ever more complex tasks at the same time

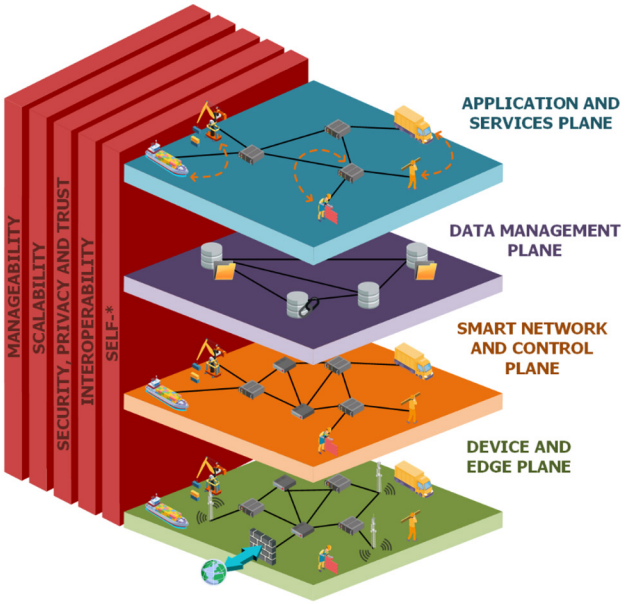

Fig. 1: Balancing Power Consummation vs. Performance

with less and less energy usage required. The circuit design and optmization have to be innovative for this delicate balance.

Environmental Impact and Sustainability issues

As more people are coming to realize, there is also a larger issue of environmental impact from building out those IoT deployments. With billions of devices that will be used in the next couple of years, even small gains in energy efficiency translate into massive reductions in total power consumed and electronic waste.

Fundamentals of Low Power VLSI Design.

For this reason, understanding the basic principle of low power VLSI design for the IoT application can avoid diving directly into the optimization technique. There are more sophisticated strategies that are built on these principals.[2-5]

VLSI Circuits Power Dissipation

In general, there are three main components of power dissipation in VLSI circuits.

1. This forms the Dynamic Power Consumption, due to the fact that a capacitive load is being charged and discharged during transistor switching.
2. **Static Power Consumption:** It refers to as the leakage power consumed by the circuit when it is idle.
3. At the switching time, when both PMOS and NMOS are conducting for a brief period, this power consumption occurs.

To develop effective power reduction strategies, these components should be understood.

Power Consumption Eating Key Factors

There are several important factors, which influence the power consumption of VLSI circuits. Supply voltage: Since the power consumption grows quadratically with the supply voltage, voltage reduction is a powerful energy efficiency tool all the more. Dynamic power consumption is directly proportional to the switching activity, i.e., the frequency of the transistor state changes. Thus, the power consumption due to charging and discharging of larger size capacitive loads is high. Shrinking transistor sizes make leakage currents an increasing percentage of the overall power consumption. The power efficiency of VLSI circuits is primarily dependent on the ultrahigh precision of manufacture of the semiconductor industry. The processes associated with lower power have smaller processes, and the price is the increase leakage currents.[6-7]

Power optimization and Design Hierarchy

Optimization of power at multiple levels of VLSI design abstraction are as follows:

Range from High level Architectural decisions and Power management Strategies till System Level. It works on Energy efficiency of computational algorithms (Algorithm Level). Circuit Level: Addresses transistor level optimizations and low power circuit techniques. Layout and physical design considerations for power reduction are addressed on the physical level.

The effective low power design at these level requires a holistic approach. Given the desire to make ever more energy efficient IoT devices, researchers and engineers are continuously pushing the boundaries of low power VLSI design. These advanced methods allow a power reduction that was previously considered impossible, but which meet or exceed performance.

Dynamic Voltage and Frequency Scaling (DVFS)

DVFS enables the processor's voltage and frequency to be dynamically adjusted. Such an adaptive approach allows for optimization of power consumption on a real time basis.

1. The system constantly monitors the amount of computations placed on the processor.
2. Performance Assessment is formed based on the monitored workload and the level of the required performance.
3. Dynamic voltage and frequency adjustment: Processor voltage and frequency are scaled dynamically in order to match performance requirements with power consumption.

Emerging Technologies Ultra Low Power IoT Devices

Due to increased demand of energy efficient IoT devices, researchers have started exploring the novel technology for the revolution of low power VLSI design. However, with the current, fast evolving IoT hardware and the increasing deployment of these emerging solutions in real product designs, they can spawn dramatic improvements in energy efficiency and expose the next generation of IoT hardware.[8-9]

Beyond-CMOS Technologies

CMOS technology has proved to be a work horse of VSLI design for years while consequently several new materials and device structures have been investigated to get round the limitations of silicon based traditional transistors. For the next generation of IoT applications to fly, ultra low power IoT (Internet of Things) devices are essential as they need to survive on very limited energy sources for prolonged periods remotely in places which are difficult to reach. With the objective to consume very minimal power yet should be functional, these devices can be used across a wide variety of applications including healthcare monitoring, environmental sensing, smart cities, industrial automation, and so on. At the same time, there is always a need for the low power devices, and hence new emerging technologies have developed to make energy efficient solutions for the IoT systems (Table 1).

Advancement of semiconductor materials and fabrication processes is among the key technologies that power ultra-low power IoT devices. New material such as gallium nitride (GaN) and silicon carbide (SiC) have begun to complement the traditional silicon based transistors that are now providing better power efficiency and heat dissipation than the silicon based transistors. By utilizing these materials, switching speeds can be faster and energy consumption can be lower which is particularly crucial for IoT devices which are designed to remain on and operate continuously or for extensive periods of time on minimal power. Energy harvesting is another emerging technology that allows IoT devices to get energy from their surroundings (solar, vibration, thermal, RF, etc.) for enabling long term continuous sensing. Energy harvesting techniques that can reduce or eliminate the need for external power supply or battery can make devices truly autonomous and sustainable. Small scale energy harvesters can be integrated into IoT devices as these can continue working without battery replacement as required in applications such as environmental monitoring or wearable health devices.[10-11]

Additionally, ultra-low power communication protocols are an important component of building energy efficient IoT devices themselves. Cost effective but challenging to operate, new communication technologies such as Low Power Wide Area Networks (LPWAN), Bluetooth Low Energy (BLE) and Zigbee allow IoT devices to communicate over long distances or remain connected and consume minimal power. The

Table 1: Advancement of semiconductor materials and fabrication processes

Challenge	Description	Impact
Power Consumption in IoT Devices	Reducing power consumption while maintaining performance is a significant challenge for IoT devices.	Increased power consumption can reduce battery life and affect device efficiency.
Design Complexity in Low-Power Circuits	Designing low-power circuits requires managing trade-offs between speed, area, and power.	Complex designs may increase development time and lead to performance issues.
Integration of Multiple Functionalities	Integrating various functionalities like sensing, processing, and communication in a single chip.	Integration complexity can result in increased size, power consumption, and cost.
Thermal Management in VLSI Design	Managing heat dissipation in compact IoT devices to ensure stable operation.	Thermal issues can lead to reduced reliability and damage to components.

energy consumptions in idle and active states have been optimized using these protocols to fit with very long distance communications in cost effective manner, making them suitable for IoT applications. In addition, approaches for power efficient hardware design are being developed to reduce power even further. Dynamic voltage and frequency scaling (DVFS) in which the operating voltage and frequency of the chip are adjusted dependent on the workload, as well as clock gating where the clock signal to portions of the chip are disabled for which are not in use and thus save power.

In short, technological advances in the area of semiconductor materials, energy harvesting methods, low power communication protocols along the way with efficient design of hardware are pushing the boundaries of ultra low power devices on the IoT. Using these innovations a new generation of energy and resource efficient IoT devices can be deployed reliably at the lower power and size budgets needed to support rapidly expanding demand from both industries and end consumers for sustainable, autonomous systems. As these technologies mature, the number of opportunities for ultra-low power IoT devices will increase, and the applications of these technologies will become even more varied (Figure 2).[12-17]

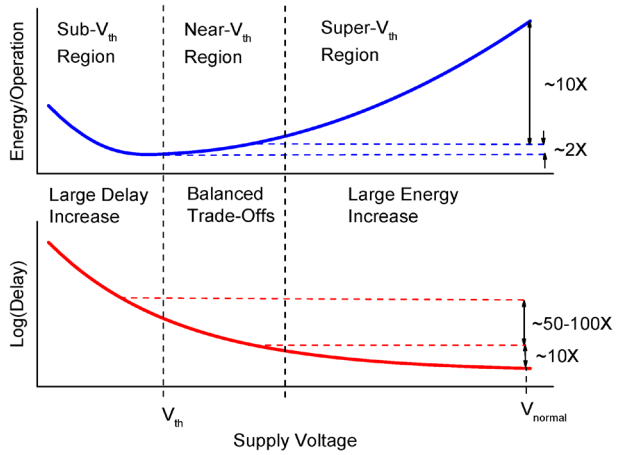

Fig. 2: Tunnel Field-Effect Transistors (TFETs) characteristics

Tunnel Field-Effect Transistors (TFETs)

Tunnel Field Effect Transistors (TFETs) are becoming significant in high speed and low power electronics as a promising alternative device to traditional MOSFETs (Metal Oxide Semiconductor Field Effect Transistors). The main difference between MOSFETs and TFETs is that TFETs are operated on the quantum tunneling rather than via conventional thermal activation mechanism in MOSFETs. The tunneling phenomenon makes TFETs operate at much lower voltages as compared to conventional FETs, making them highly attractive for power – efficient electronics, specifically for IoT, mobile computing, and low – power logic circuits.[18-20]

Current conduction in a TFET is due to quantum mechanical tunneling effect. The application of the gate voltage causes the source channel to be placed in close proximity and the carrier injection resulting from the tunneling instead of the traditional drift mechanism as it exists in MOSFETs. As a result, a much reduced value of the subthreshold swing, a key figure of merit for low power operation, is achieved. Theoretically, TFETs can achieve subthreshold swing below the ideal limit of 60 mV/decade at room temperature, which is lower than MOSFETs of 70-80 mV/decade. The power consumption is very critical in low voltage, low power applications, and this makes TFETs very suitable in such applications (Figure 3).[21-26]

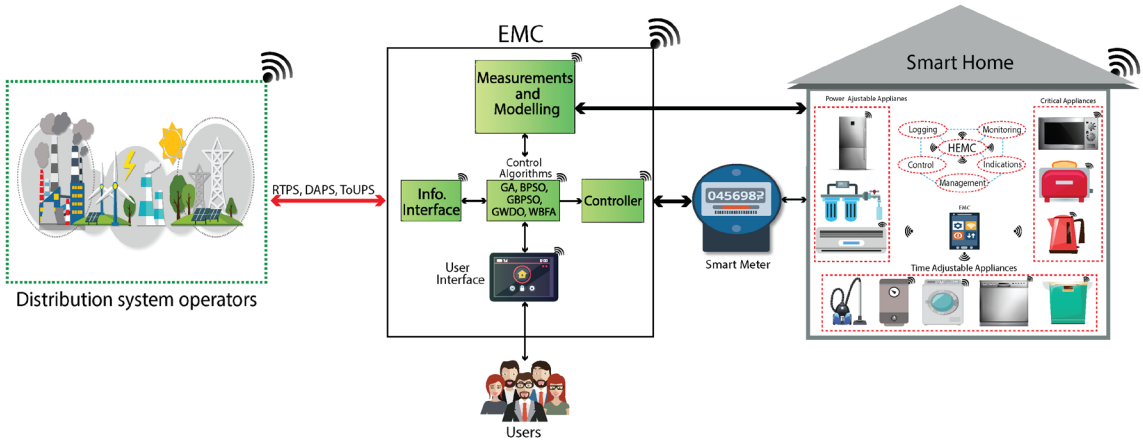

Fig. 3: Current conduction in a TFET

Table 2: MTJ Low read/write energy non volatile memory elements

Solution	Description	Benefit
Dynamic Voltage and Frequency Scaling (DVFS)	DVFS adjusts the voltage and frequency according to the workload, reducing power consumption during idle times.	Helps balance performance and power consumption by adapting to the system,Äôs needs.
Low-Power CMOS Technology	Using low-power CMOS technology allows for the reduction of static power consumption in the circuits.	Reduces the overall static power consumption of IoT devices, extending battery life.
Power Gating and Clock Gating	Power gating and clock gating techniques selectively turn off idle components to save energy.	Minimizes energy consumption by selectively turning off unnecessary parts of the system.
Energy-Efficient Design Techniques	Design techniques like multi-threshold CMOS and sub-threshold operation minimize energy usage while maintaining functionality.	Improves energy efficiency without compromising device performance or speed.
Advanced Fabrication Processes	Advanced fabrication techniques, like FinFET and SOI technologies, provide lower power consumption and higher performance.	Enhances device performance while ensuring energy savings due to more efficient transistor switching.

Particularly, TFETs also offer better performance at lower supply voltage than MOSFETs. As the semiconductor manufacturing process continues to scale transistor sizes, the demand for devices which can function well at low operating voltages is increased. This role is very well suited for TFETs since they continue to drive high current even at reduced gate voltages, which significantly helps to overcome two key problems associated with modern integrated circuits: power consumption and heat dissipation.

However, in practical implementations, they suffer from some issues. The mechanism of tunneling is highly critical with respect to the source and channel materials used, as the goal is to achieve deserving tunneling whilst preserving device performance. Generally, TFETs are fabricated by using more complex material engineering, including using narrow bandgap semiconductor materials such as germanium (Ge) or III – V materials to increase tunneling efficiency. Furthermore, TFETs performance can be impaired, for example due to process variations, which have to be prevented by a careful control during fabrication.[26-30]

Generally, TFETs show interesting prospects to improve performance of electronic devices in the sense where power efficiency takes a premium. Although such issues can significantly reduce the prospects for commercial deployment of TFETs within the near future, more research into advances in material properties, fabrication processes and device architectures may soon result in TFETs becoming a common feature of the next generation of ultra-low power electronics and high speed digital circuits.

As a demand for energy-efficient IoT devices keeps on growing, researchers are exploring novel technology that promises to revolutionize low-power VLSI design with its features including MTJ Low read/write energy non volatile memory elements, Logic in memory architecture and potential in improving the write energy efficiency. Emerging solutions for these problems could provide a significant improvement in energy efficiency as we move towards the next generation of IoT hardware (Table 2).

Thus, a proposal is done of using the neuromorphic computing based on the structure and function of the biological neural network to achieve the energy efficient processing in the IoT devices. As low power consumption for certain types of computation as possible. Successful ability to handle noisy and incomplete data On device learning, and ability to self adapt Efficient neuromorphic hardware architectures to develop Hardware architectures with coherent programming models, tools and languages Integrated with traditional computing paradigms represents the ultimate goal for many IoT applications, which are to create self sustaining devices that may last for ever without external power source.

Conclusion: Low Power VLSI Design to Shape the Future of IoT

The need for low power VLSI design is becoming an important need, as we are moving towards the edge of a new era of IoT technology. These will be, as you have read in the article above, only the beginning of what will surely become a technological revolution in designing and producing IoT energy efficient devices. Such an insatiable area is fertile for newer, more emerging VLSI low power design space for the IoT space —from circuit level to architectural innovation— and beyond CMOS domain in quantum computing. As researchers and engineers push farther into what's possible, we can expect IoT devices to become more and more energy efficient and capable, as well as more secure, and able to accommodate all sorts of needs for our connected world. But the potential rewards are great, the challenges ahead are large. To enable such IoT technologies to really change every bit of existence, we address the issues of scaling costs, security concerns, and the need for self powered operation. The world will feel the benefits of energy efficient IoT hardware across smart cities, precision agriculture, healthcare, industrial automation, and far beyond. We are looking forward to the future, and we know that future of low power VLSI will keep persisting its effect in future IoT. All of this, we can speed it up by creating collaboration between academia, industry, and open source companies to establish this marketplace and distribute the gain of ultra low power IoT devices to everyone. Across the board in VLSI design, relentless search for energy efficiency is already underway towards truly sustainable, intelligent, and ubiquitous IoT technology.

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