

Photonic Integrated Circuits in Next-Generation Optical Communication Systems: A Comprehensive Review of Design, Fabrication, and Emerging Applications

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ABSTRACT

Photonic integrated circuits (PICs) are transforming the next-generation optical communications systems due to their ability to provide ultra-high data rates, compact systems, and extremely low power consumption. PICs can solve this problem because they will support the ever-increasing amount of data traffic caused by cloud computing, 5G/6G networks, and AI workloads in a simple, clean, and energy-efficient way. In this review, the author provides an in-depth review of the PIC landscape in terms of main design methodologies, mature and advanced fabrication processes as well as diverse integration strategies on the main material platforms, silicon photonics, III-V semiconductors, and lithium niobate among others. We discuss critical state-of-the-art components such as the modulators, photodetectors, multiplexers and the coherent transceivers, their applications in data center interconnects, long-haul transmission and reconfigurable optical networks. The next wave in quantum technologies The emergence of quantum technologies, quantum LiDAR, quantum biomedical diagnostics, quantum neural networks and their applications are also discussed. Other important aspects of key design and manufacturing issues, including the relationship of thermal stability, coupling losses, yield scalability and heterogeneous integration, are also said in details. The paper ends with future analysis of research on the fields of reconfigurable architecture, AI-assisted photonic design, and monolithic photonic-electronic co-integration, in which PICs play a pivotal role as a foundation piece of technology to the high-performance, broadband communication and beyond.

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INTRODUCTION

The current global trend of exponential increase in volume of data traffic, caused by the rise in cloud computing, video-on-demand services, IoT ecosystems, and other emerging technologies such as artificial intelligence (AI), augmented reality (AR), and virtual reality (VR), is posing bandwidth and latency challenges to modern communication networks unprecedented in nature. Conventional electronic interconnect and discrete optical systems are not keeping pace with these new requirements, because of the current limitation in speed and power efficiency, as well as integration

density. The development of 6G, which constitutes a step beyond 5G, and roll-out of hyperscale data center facilities and edge computing networks, have led to an increasing demand in medium-capacities, low-latency, and energy-efficient communication technologies.

The emergence of Photonic Integrated Circuits (PICs) has seen the chance to have most of the optical devices needed such as laser, modulator, waveguide, multiplexer, and photodetector, mounted on the same chip, and this aspect has seen it receive a huge boost in terms of popularity. Similar in functionality to electronic integrated circuits (ICs), PICs use photons (light) instead



Fig. 1: Overview of the Photonic Integrated Circuit (PIC) Ecosystem

of electrons in order to carry out high speed circuit signal processing and data transmission. Compared to traditional discrete optical systems that require fiber splices and large packaging, PICs have quite a number of benefits that include; more minimal insertion loss, smaller footprint, increased system reliability, and reduced cost per-bit transmission. Such common fabrication platforms include silicon-on-insulator (SOI), indium phosphide (InP), silicon nitride (SiN) and more recent lithium niobate on insulator (LNOI) each with unique possibilities of active and passive photonic device integration. Fig. 1 illustrates that the PIC ecosystem is spread over the design, fabrication and application areas where each area is supported by specific technological pillars.

Overview of the Photonic Integrated Circuit (PIC) ecosystem highlighting the three main stages: Design, Fabrication, and Application, along with representative elements in each stage.

This review seeks to give a substantial and systematic review of Photonic Integrated Circuits and their contribution to realising next generation optical communication systems. Design approaches such as simulation, layout optimization and measures of performance will be examined in the paper and so too will fabrication techniques spanning CMOS-compatible photonics through to hybrid and heterogeneous integration technologies. Moreover, we discuss the methods of integration that make the photonic-electronic convergence and co-packaging possible. Lastly, we cover the hot new applications of capabilities such as data centers interconnects and metro networks as well as quantum photonics, LiDAR, biomedical sensors, and neuromorphic computing. It is concluded by critically discussing contemporary challenges on thermal management, variability of yields, and reconfigurability,

alongside so positing future directions that encompass AI-aided photonic design and scalable, reconfigurable photonic architectures and systems, the latter of which have high performance potential.

PHOTONIC INTEGRATED CIRCUIT FUNDAMENTALS

Photonic Integrated Circuits (PICs) make use of physics of light to high-speed signal processing and transmission on a footprint (chip) scale. To comprehend the workings and the building blocks of PICs is of paramount importance to appreciate their working and application in the current optical communication systems.

Operating Principles

The key element contained in a PIC is the concept of waveguide-based lights transmission, which are miniaturized optical waveguides that were produced in a semiconductor substrate and which confine and propagate photons. These waveguides have the same application as metal interconnects in the electronic circuits but with much lower losses at high data rates. The chip may be seeded with the optical signal through grating couplers or edge couplers and is subsequently propagated through diverse functional photonic devices.

The basic optically manipulated signals on PICs are threefold:

- **Modulation:** The information is coded into the optical carrier in the following way: The amplitude, phase or frequency is altered. This is usually done with the help of electro-optic or thermo-optic modulators. Mach-Zehnder Interferometer (MZI) is a common amplitude and phase modulator structure.
- **Filtering:** Optical filters are significant in wavelength sorting to channel, and also, to

signal processing. Filter designs Centering filter Components: The filter centers usually employ ring resonators or Bragg gratings as the compact and wavelength-selective filtering component. Process: The filter centers are based on a ring resonator or Bragg grating.

- **Multiplexing/Demultiplexing:** These enable the combination of multiple optical signals at different wavelengths (WDM) or separation (demux) on the same waveguide with the result that the optical data carrying capacity of the optical link is increased. The most used integrated solutions to this end include arrayed waveguide gratings (AWGs) and echelle gratings.

These functions are made possible by tight control of the refractive index contrast, waveguide geometry and material so as to determine the functioning parameters like insertion loss, bandwidth and crosstalk.

Key Components

Current PICs consist of an array of several active and passive optical devices with each component of the optical signal chain doing a dedicated task. Major functioning components that make high-speed signal manipulation in PICs. includes:

Mach-Zehnder Interferometers (MZIs): Mach-Zehnder Interferometers are the equivalent of two arms of a light interferometric setup. The optical path length in one arm can be varied by the application of an external voltage (electro-optic effect) allowing amplitude and phase modulation to be applied to the output pattern of interference. MZIs are of significant interest in modulators, switches and filters.

Ring Resonators: These small circular waveguides resonate at well-defined wavelengths, that is why they are applied to filter, switch, or sense wavelengths. They are of a high quality (Q) and small footprint dimensions that makes them highly integrated in WDM systems.

Electro-Optic Modulators: Electro-optic devices make use of electro-optic materials (e.g. lithium niobate, silicon-organic hybrids) to dynamically change the

refractive index in the presence of an electric field, thereby altering the phase or intensity of the optical signal applied to it. The need to support even higher data rates than 100 Gb/s demands high-speed modulation.

Photodetectors are used to convert optical signals into electrical current which can then be manipulated. To increase the speed of detection in PIC, Ge-on-Si and InP photodiodes have been implemented. They can be easily connected with transimpedance amplifiers (TIAs) to make effective receiver front ends.

Couplers and Splitters: Couplers and splitters are used to split and combine optical power between waveguides and are passive components. Directional couplers, multimode interference (MMI) couplers, and Y-branch splitters are the common interconnection structures used in PIC to control signal distribution.

All of these components need to be highly designed and optimized so as to minimize loss, have high bandwidth as well as reliable functioning. They can be integrated to form a monolithic or hybrid platform which makes it possible to provide complex photonic systems with reduced footprints and high performance to a variety of optical communication applications. Table 1 contrasts the major photonic elements based on insertion loss and its physical area affecting design trading.

Functional components of a Photonic Integrated Circuit (PIC), including Mach-Zehnder interferometers, ring resonators, electro-optic modulators, photodetectors, and couplers.

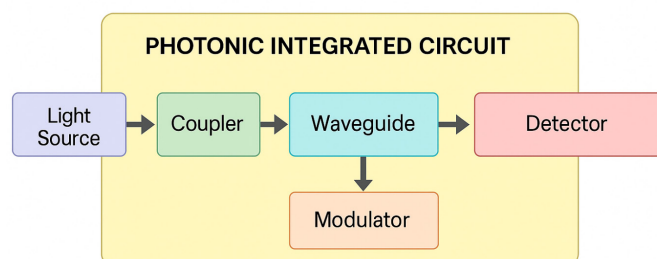


Fig. 2: Functional components of a Photonic Integrated Circuit (PIC)

Table 1: Insertion Loss and Footprint of Key PIC Components

Component	Platform	Insertion Loss (dB)	Footprint (mm ²)	Notes
MZI Modulator	Silicon	3-6 dB	-0.5-1.0	Requires driver circuits
Ring Resonator Filter	Silicon/SiN	< 1 dB	-0.01-0.05	Compact but thermally sensitive
AWG Demux	InP / Silicon	3-5 dB	1.0-2.5	Footprint depends on channel count
Photodetector (Ge-on-Si)	Silicon	< 1 dB	-0.1-0.2	Integrated with TIAs

DESIGN METHODOLOGIES

Photonic integrated Circuits (PIC) design involves designing in a multi disciplinary fashion spanning optics, electronics, material science and semiconductor processing. This paragraph presents the top-down design flow, key performance parameters, and the new significance of photonic-electronic co-design to high-performance optical systems.

Design Flow

PIC design starts with the functional design at the schematic level, where schematic designers list the functional components (e.g., modulators, couplers, detectors) and the interconnection of these components using hardware description languages or photonic design software. This functional abstraction is mapped into size, geometry, spacing, routing, physical dimensions at layout-level where arm lengths are specific, waveguide shapes are specific, distance between them is specific, and the routing is clearly defined.

Photonic EDA tools Photonic heavy flows exist for PIC design, which permits simulation, layout, and verification of photonic elements. Among the popular tools there are:

- Lumerical INTERCONNECT and FDTD (by Ansys): so-called general purpose software, widely used to simulate electromagnetic behavior and optical wave propagation, as well as time-domain responses of photonic devices and circuits.
- IPKISS and Luceda Photonics Suite: Provides a parameterized cell (PCell)-based programmable design foundry, which facilitates the reuse of the components and fast design turnaround.
- Synopsys OptoCompiler: The layout generation and schematic capture, along with process design

kit (PDK) compliance are integrated into a silicon photonics-compliant flow. It encourages simulation at the circuit level, layout-versus-schematic (LVS) analysis and automatic DRC (design rule checking). Manufacturability is often ensured with the aid of foundry-specific PDKs that are foundry-specific such as platforms offered by AIM Photonics, IMEC, or GlobalFoundries.

These consist of pre validated building blocks and technology files that drive fabrication within the tolerances of a certain photonic process node. Figure 3 shows the global PIC development flow, i.e., the specification, layout, and verification.

Generic design flow for Photonic Integrated Circuits, from schematic capture and simulation to layout generation and verification using photonic EDA tools and foundry-specific PDKs.

Performance Metrics

The measurement of the figure of merits used to determine the effectiveness of a PIC design constitutes several critical values that define its application to specific elements:

Insertion Loss (IL): Optical power loss due to the propagation, scattering and coupling. Several IL reduction strategies are necessary in preserving signal strength particularly in architecture involving cascades.

Extinction Ratio (ER): It is a parameter that quantifies the extent of modulation, by which the power of the on and off optical state is apportioned in turn. Large ER is essential to support good signal modulation as well as high optical SNR.

Bandwidth: It defines the transmission of data capacity of the PIC. It depends on the wavesguide dispersion, the resonator Q-factors and the speed of the device. A

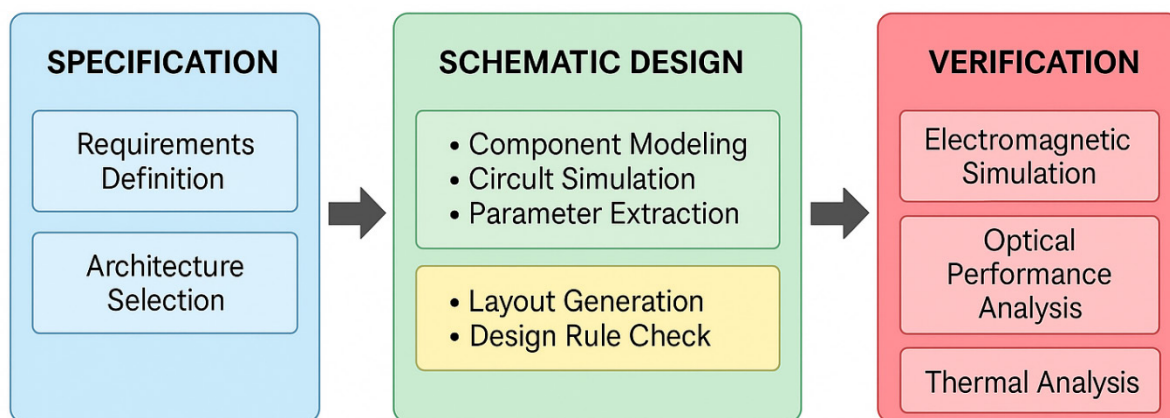


Fig. 3: Photonic Integrated Circuit (PIC) design flow

design aiming to support 100+ Gb/s data rates must be capable of supporting wide 3-dB bandwidths.

Footprint: Area of chip on which a photonic device takes images. It allows a smaller footprint that allows greater integration density, lower-cost wafer consumption and smaller packing.

Other factors are thermal stability, polarization sensitivity, and variability during the process. Multi-physics models (electro-optical and thermal, thermal and mechanical) are used by designers to find the optimal performance parameters early in the design process.

Co-Design with Electronics

Performance bottlenecks in most optical systems tend to migrate to the photonics electronics interface. Therefore, it has become a trend to co-design photonic and electronic components-also termed as Opto-Electronic Integrated Circuits (OEICs).

In OEICs the photonic components (e.g., modulators, detectors) are closely integrated with electronic drive, amplifiers and control logic all on the same die, or in the same housing. The assimilation enables:

- The minimum parasitic capacitance and inductance and superior signal integrity to higher frequency.

On chip power reduction and interface matching.

- Enhanced cooling and space deficient, needed in an embedded or data center system.

Some of the technologies that will allow co-design are heterogenous integration (e.g. bonding InP devices to CMOS wafers), 3D integration using through-silicon vias (TSVs), and co-packaged optics (CPO), optical and electronic dies are assembled together into the same module.

Advanced simulation environments Cadence Spectre, Synopsys PrimeSim and Lumerical electrical-optical co-simulation environments are used to simulate the signal paths, jitter, timing margins and interaction of noise across the entire opto-electronic stack. It is this kind of holistic design method that would be used to realise next-generation high-speed interconnects, optical transceivers and neuromorphic photonic systems.

FABRICATION TECHNOLOGIES

Photonic Integrated Circuits (PICs) are fabricated through a highly precise process of combining optical structures at a micro- and nano-scale level via unique processes with regard to semiconductor manufacture. This section examines the prevailing material platforms, fabrication

methodologies, and some of the major issues related to yield, tuning, and packaging.

Material Platforms

The Photonic Integrated Circuits are produced on a range of material platforms, and different opportunities are unique to a given application. The most developed and CMOS-compatible system is silicon photonics on silicon-on-insulator (SOI) wafers. It has high refractive index contrast to dense integration and can propagate efficient passive components and modulators. It is however lacking in efficient light emission owing to the fact that silicon has an indirect bandgap which requires the hybrid integration of silicon with the III-V materials to produce on chip lasers. Monolithic integration of active photonic elements Monolithic integration of active elements (transmission and reception) of a photonic device, like lasers and modulators, and photodetectors can be achieved in III-V semiconductors, including indium phosphide (InP) and gallium arsenide (GaAs). InP is very applicable in high-performance coherent transceivers whereas GaAs is commonly applied in ultrafast photodetectors and electro-absorption modulator. Silicon nitride (SiN), because of its ultralow propagation loss, has many applications in high-Q resonators, biological sensors, and sub-THz and nonlinear optics circuits, especially in the visible and near-infrared. Lithium niobate on insulating (LNOI) is a system in an early development stage that shows good electro-optic and nonlinear properties. It enables high-speed low-voltage modulation and is proving useful to enhance the potential of advanced applications of quantum photonics, frequency conversion, and integrated electro-optic systems. Such a combination of the platforms provides an elastic platform to scalable high-performance-photonic integration. The table 2 illustrates the modulation bandwidth of different PIC platforms which can be applicable to high-speed optical communications.

Fabrication Processes

Photonic Integrated Circuits manufacturing involves drawing upon the traditional semiconductor processing technology as well as the knowledge of integration strategy to produce compact, high-performance optical functionality. Silicon photonics is mostly built on CMOS-compatible processes, including the use of familiar semiconductor processing equipment, deep-ultraviolet (DUV) lithography, plasma-enhanced chemical vapor deposition (PECVD), and reactive-ion etch (RIE). The processes enable economical and scalable fabrication, frequently in commodity CMOS fabs, and employ

Table 2: Comparison of Modulation Bandwidths Across Material Platforms

Platform	Modulation Type	3-dB Bandwidth	Typical Device	Reference
Silicon Photonics	Carrier Depletion (PN)	10-40 GHz	Mach-Zehnder Modulator (MZM)	Thomson et al., 2016
InP	Electro-Absorption (EAM)	40-70 GHz	InP EAM	Hattori & Kurimura, 2015
LNOI	Electro-Optic (Pockels)	60-110 GHz	LNOI MZM	Wang et al., 2020 (Nature)
SiN	Thermo-Optic	< 1 GHz	Ring Resonator Filter	Bogaerts et al., 2012

well-developed photonic process design kits (PDKs) with characterised parts libraries and guidelines. But overlapping multiple materials with a single material platform does not produce all the required optical capabilities, including the efficient production of light, packaging and manipulation, and detection. Thus hybrid integration techniques and wafer bonding are used to combine complementary materials. This encompasses the combination of III-V gain medium (e.g., InP) with silicon substrates by adhesive bonding, direct wafer bonding and transfer printing. These hybrid techniques will facilitate co-integration of active photonic components like lasers and optical amplifiers with passive bandwidth-rich silicon waveguide circuits thus to increase functionality and extend the range of applications of PIC in high speed and coherent optical communication systems.

Yield, Tuning, and Packaging Challenges

The yield variability due to fabrication imperfections is one of the major obstacles in the large-scale photonic integration. High Q resonators, narrow waveguides, and photonic devices, in general, are rather sensitive to dimensional variations and process-induced non-uniformities, which can cause serious shifts in operating wavelengths and higher insertion loss, and poor performance consistency across wafers. To counter these problems, post-fabrication tuning mechanisms are most of the time applied. Thermal tuning with integrated microheaters is the most used tuning technique because of its simplicity and generous tuning range but also brings about an additional consumption of power and crosstalk of heat. Faster responses, with less thermal overhead can be achieved using alternative methods of carrier

injection and electro-optic tuning which have greater complexity requirements in terms of integration. Based on the data obtained in Table 3, both electro-optic and MEMS tuning have higher efficiency and speed data compared to the traditional tuning technologies that are thermally related.

Also, there are special difficulties in packaging PICs, as opposed to electronics. Optical photonic packaging has to provide sub-micron alignment finesse to optical fibres, to handle active-component thermal dissipation and to provide optical and electrical interconnections in a small form factor. Packaging of PIC has been found to be very expensive and complex that they may take the lead in the overall system cost. To deal with this, new solutions are being created consisting of fiber-array coupling, flip-chip bonding, and photonic interposers and integrated photonic sockets that improve scale and alignment tolerances of photonic interconnects along with making the mass fabrication process becomes simpler.

5. INTEGRATION ARCHITECTURES

The design employed to combine photonic components with other photonic elements, or with electronics has a dramatic effect on the performance, scalability and cost of Photonic Integrated Circuits (PICs). This implementation will give examples of the major integration methodologies, such as monolithic schemes, co-packaged or chiplet-based architectures.

Monolithic vs. Hybrid vs. Heterogeneous Integration

Monolithic integration is a method in which all photonic components, active and passive are fabricated on

Table 3: Tuning Efficiency Comparison: Thermal vs. Electro-Optic Methods

Tuning Method	Power Consumption	Speed	Efficiency	Scalability
Thermal Tuning (Resistor)	20-50 mW per device	μs-ms	Low ($\Delta n \sim 10^{-5}/\text{mW}$)	Limited by thermal crosstalk
Carrier Injection (Si)	~1-5 mW	ns-μs	Moderate	CMOS compatible
Electro-Optic (LNOI)	<1 mW	ps-ns	High ($\Delta n \sim 10^{-4}/\text{V}$)	Excellent (non-thermal)
MEMS Actuation	~μW	ms	High (mechanical Δn)	Good but complex to fabricate

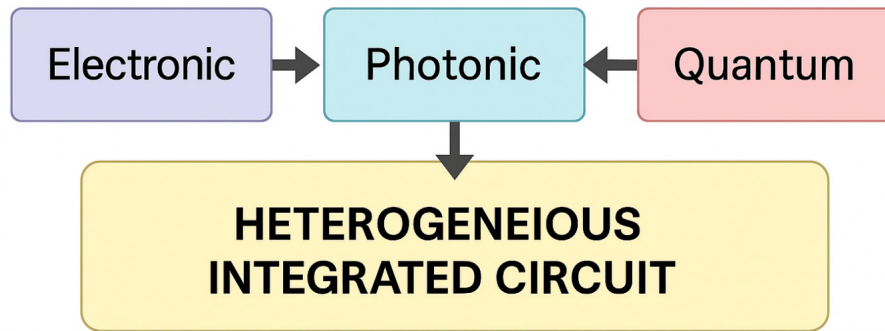


Fig. 4: Integration of different platforms

one and the same substrate within one and the same material system. Silicon photonics leads as an example with passive waveguides and modulators of the same SOI wafer. Although this approach offers very high precision alignment and compatibility with CMOS Processing, it lacks options because silicon is not efficient to undertake functions such as light production or light detection of specific wavelengths.

In order to address these material shortcomings, creating a hybrid integration initiative can merge several dissimilar photonics materials, each of which is customized towards certain capabilities, by bonding or epitaxially growing them onto a shared platform. As an example, it is possible to bond indium phosphide (InP) lasers to a silicon photonic platform to permit the efficient on-chip generation of light which can be used where the silicon circuit would otherwise be passive. As shown in Figure 4, heterogeneous integration has also led to the convergence of these components, or rather a blending of electronics, photonics and quantum hardware components.

Figure 4. Illustration of hybrid and heterogeneous integration of dissimilar material platforms (e.g., InP, LNOI, SiN) into a Unified photonic system.

Heterogeneous integration is a further development of hybrid integration, where dissimilar materials (InP, GaAs, SiN, LNOI) are intimately co-fabricated or bonded, at the wafer-level. This enables them to be used together with high-performance active devices and dense silicon based photonic circuits to create compact and practical systems of photonics. Heterogeneous techniques provide the optimal combination of scalability due to the silicon processes and the extensive functionality of III-V materials, although complex techniques are needed to align, bond and temperature regulate the structures.

Photonic-Electronic Co-Packaging

With data rates constantly rising, electrical interconnection between photonic and electronic

components becomes a weak spot because of the parasitic losses and signal degradation. Another approach to this problem is photonic-electronic co-packaging, which tries to pack optical and electronic dice into the same package, or even on the same substrate. PICs also allow integrated and fast coherent transceivers that can operate in long-haul and metro networks, see Fig. 5. Co-packaged optics (CPO) involve placement of photonic chips next to, or on top of, electronic processors or switch ASICs, as such, reducing the length of interconnect, and improving signal fidelity. This architecture is particularly important in data center switches where next generation 51.2 Tbps systems are required to have interfaces with exceptionally low-loss and low-latency. There is also increased thermal efficiency and reduced board routing in co-packaging creating smaller and less power-consuming systems.

Silicon interposers, embedded waveguides, micro-bump bonding and through-mold vias (TMVs) are some of the integration strategies used in co-packaging. The basis of standardism on package formats, alignment tolerances, and thermal interface material is becoming useful to facilitate industrial volume, in particular to streamline packaging.

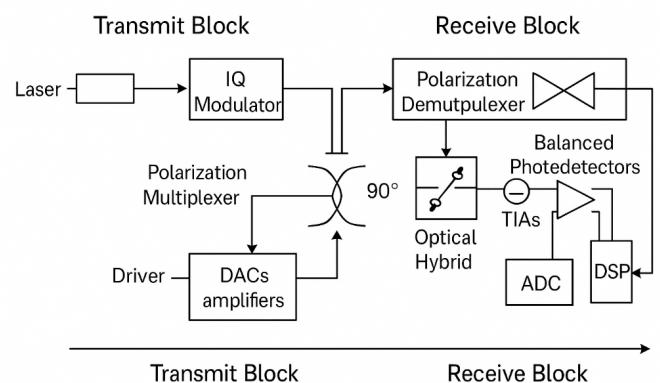


Fig. 5: PIC-based Coherent Transceiver Architecture

Block-level architecture of a PIC-based coherent transceiver, showing integrated modulators, drivers, TIA, DSP, and local oscillators.

Advanced Interconnects

With the increase in complexity of optical systems, new interconnect architectures are needed to provide the necessary signal routing, chiplet communication, and vertical integration.

Another promising avenue is optical I/Os to chiplets, in which photonic interconnect is used in lieu of electrical buses to communicate between chip or die-to-die. In this approach, disaggregated computing and reconfigurable hardware architecture are possible by interconnect high-bandwidth with low-latency, with less electromagnetic interference (EMI).

The other killer enabler is the 3D integration via through-silicon via (TSVs) and micro-transfer printing. With these technologies the photonic and electronic layers can be stacked in the z-dimension at much higher functional densities without need to repackage and heighten the chip area. All control electronics, lasers and photonic routing layers can be on separate planes and behave as a single system in 3D PICs. Thermal dissipation, coupling efficiency between different layers, and alignment accuracy are challenges still to solve but 3D integration is the future of high performance, compact photonic systems.

USE CASES AND DEPLOYMENT SCENARIOS FOR PICs

Photonic Integrated Circuits (PICs) have become a game-changer in the optical communication systems in the real world due to the ability to make optical solutions high-performance, compact, and energy-efficient in various applications. PICs are installed in CWDM/DWDM transceivers and in coherent modules in hyperscale data centers as interconnects requiring near-zero latency with minimal power draw to run at multi-terabit interconnect characteristics. In long-haul and metro networks, the PICs support tunable lasers, wavelength and integrated correlated detection, which enables wavelength flexibility, high-order modulation formats, and DSP-improved long-haul signal optimization. PIC-based reconfigurable optical add-drop multiplexers (ROADMs) use optical switched and routed networks to achieve dynamic management of lightpaths over a network without going OEO; they are reconfigurable at the optical layer to enhance flexibility in the next generation of elastic optical networks. Moreover, the wireless optical communication systems, such as LiFi and free-space optics (FSO) use PICs to allow for compact on-board combinations of beam steering, adaptive modulation, and light sensory components, providing the capacity of high-speed optical connection to untethered, indoor, or moving operational conditions.

All these deployment scenarios show that the PICs are rapidly maturing and becoming more versatile in terms of its use in wired as well as wireless communication systems.

CHALLENGES AND RESEARCH GAPS

Nevertheless, due to the spectacular advancement experienced in photonic integration, there remains a set of technical and infrastructural hurdles that still hamper scalability and wide proliferation of Photonic Integrated Circuits (PICs). Among the key challenges, there is the necessity of thermal management because the change of temperature-related refractive index may result in the wavelength drift and the degradation of the performance of high-density photonic circuits. Post-fabrication circuit trimming is often done using thermal tuners like integrated microheaters which have high static power consumption and also result in thermal crosstalk which is undesirable to scale circuits. There is a demand to explore the other low-power tuning mechanisms, specifically carrier injection, MEMS actuation, and phase-change materials in research in order to improve tuning efficiency and rapidity. One more fatal flaw is that there is no standardization of photonic design kits (PDKs). Existing PDKs are wildly different between foundries and usually, not many complete models of the active devices exist, resulting in a lack of portability of designs and slower time spent developing. Design reusability and rapid prototyping can be found in small measure without the consolidation of co-simulation with electronics and thermal PDKs, that insisted upon being distributed as multi-physics, unified and open source.

Of equal concern are the topics of scalability, reconfigurability and foundry access. The current production of PICs is specific-purpose oriented, and hence they do not support general-purpose programmability. Newer architectures, such as reconfigurable photonic meshes, optical FPGAs, and neuromorphic photonic processors have potential, but currently need more developed control solutions and software toolchains. With regards to fabrication, small access to commercial photonic foundries, particularly of more challenging materials and infrastructures such as LNOI and SiN, brings an important obstacle to academic institutions and startups. Costs, long turnaround times, and lack of affordable custom packaging solutions still prevent the iterative development and scaling that would occur with true multi-project wafer (MPW) services, though accessibility has been improved. In the development of shared fabrication facilities, uniform PDKs (process design kits) environments, and affordable packaging platforms, the greatest potential of photonic integration

in industry and research applications will ultimately be achieved.

CONCLUSION

Photonic Integrated Circuits (PICs) Photonic integrated circuits (PICs) has become one of the key emerging photonic technologies in next-generation optical networks providing the potential of ultra-high-speed, energy-efficient and significantly scalable solutions to the exponentially increasing traffic of data-driven infrastructure. PICs are driving unprecedented levels of integration and functionality on a chip-scale platform in cloud-scale data centers and metro/core transport networks, and in wireless optical communication systems, and emerging quantum systems.

The review has covered the entire PIC ecosystem, starting at the principles of waveguide-based optical signal processing and continuing toward state-of-the-art component design and material platform, fabrication and integration stacks. These are silicon photonics maturity, the structural specificity of III-V semiconductors and SiN, as well as the disruptive technologies of lithium niobate on insulator (LNOI) platforms, illustrating the technological variability in the contemporary photonic development. The related, co-design methodologies and performance metrics were also mentioned with increased interactions of photonics and electronics to attain end-to-end system optimization.

We have described how PICs are increasingly used in real world applications: supporting coherent transceivers in long-haul systems, agile switching in reconfigurable networks and compact beam steering units in LiFi and free-space optical communication. Nevertheless, significant issues still exist in thermal control, uniformity of the yields, efficiency of tuning, and scalability in packaging. In addition, non-standardization in photonic design kits and minimal access to foundries still hinders the wider adoption and innovation, especially to new entrants and academia based research.

With a projective approach, future research needs to be on enhancing reconfigurability, on the energy-efficient body that will manipulate tuning and design, on enhancing user automation and on opening the rules that will allow open-access design/manufacture flows. The new directions of AI-based photonic design, neuromorphic photonic computing, and even quantum PICs all indicate a time when a photonic integrated circuit is no longer an electronics afterthought, but a pillar on its own.

Concluding, PICs cannot be seen as a simple enhanced version of conventional optics, it is a fundamental

transition towards an integrated, scalable and intelligent system of photonics! As the technology still refines itself, it will transform the performance, architecture, and potential of optical communication, as well as information processing, at a large number of industries.

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